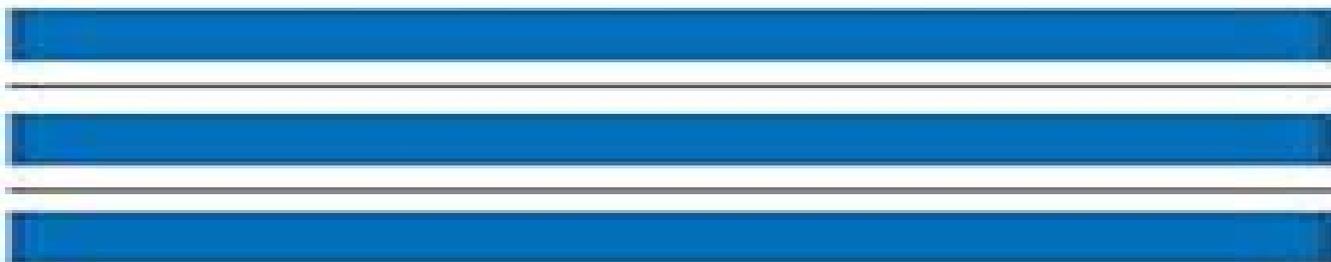

Yield Simulation for Integrated Circuits

Duncan Moore Henry Walker



Yield Simulation For Integrated Circuits

Israel Koren



Yield Simulation For Integrated Circuits:

Yield Simulation for Integrated Circuits D.M. Walker,2013-04-17 In the summer of 1981 I was asked to consider the possibility of manufacturing a 600 000 transistor microprocessor in 1985 It was clear that the technology would only be capable of manufacturing 100 000 200 000 transistor chips with acceptable yields The control store ROM occupied approximately half of the chip area so I considered adding spare rows and columns to increase ROM yield Laser programmed polysilicon fuses would be used to switch between good and bad circuits Since only half the chip area would have redundancy I was concerned that the increase in yield would not outweigh the increased costs of testing and redundancy programming The fabrication technology did not yet exist so I was unable to experimentally verify the benefits of redundancy When the technology did become available it would be too late in the development schedule to spend time running test chips The yield analysis had to be done analytically or by simulation Analytic yield analysis techniques did not offer sufficient accuracy for dealing with complex structures The simulation techniques then available were very labor intensive and seemed more suitable for redundant memories and other very regular structures Stapper 80J I wanted a simulator that would allow me to evaluate the yield of arbitrary redundant layouts hence I termed such a simulator a layout or yield simulator Since I was unable to convince anyone to build such a simulator for me I embarked on the research myself

A New Methodology for Yield Simulation of Integrated Circuits Carnegie-Mellon University. SRC-CMU Research Center for Computer-Aided Design,J. B. Khare,1989

Computer-Aided Design of Analog Integrated Circuits and Systems Rob A. Rutenbar,Georges G. E. Gielen,2002-05-06 The tools and techniques you need to break the analog design bottleneck Ten years ago analog seemed to be a dead end technology Today System on Chip SoC designs are increasingly mixed signal designs With the advent of application specific integrated circuits ASIC technologies that can integrate both analog and digital functions on a single chip analog has become more crucial than ever to the design process Today designers are moving beyond hand crafted one transistor at a time methods They are using new circuit and physical synthesis tools to design practical analog circuits new modeling and analysis tools to allow rapid exploration of system level alternatives and new simulation tools to provide accurate answers for analog circuit behaviors and interactions that were considered impossible to handle only a few years ago To give circuit designers and CAD professionals a better understanding of the history and the current state of the art in the field this volume collects in one place the essential set of analog CAD papers that form the foundation of today s new analog design automation tools Areas covered are Analog synthesis Symbolic analysis Analog layout Analog modeling and analysis Specialized analog simulation Circuit centering and yield optimization Circuit testing Computer Aided Design of Analog Integrated Circuits and Systems is the cutting edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck

Defect and Fault Tolerance in VLSI Systems C.H. Stapper,V.K. Jain,Gabriele Saucier,2013-06-29 Higher

circuit densities increasingly more complex application objectives and advanced packaging technologies have substantially increased the need to incorporate defect tolerance and fault tolerance in the design of VLSI and WSI systems The goals of defect tolerance and fault tolerance are yield enhancement and improved reliability The emphasis on this area has resulted in a new field of interdisciplinary scientific research In fact advanced methods of defect fault control and tolerance are resulting in enhanced manufacturability and productivity of integrated circuit chips VLSI systems and wafer scale integrated circuits In 1987 Dr W Moore organized an International Workshop on Designing for Yield at Oxford University Edited papers of that workshop were published in reference II The participants in that workshop agreed that meetings of this type should be continued preferably on a yearly basis It was Dr I Koren who organized the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems in Springfield Massachusetts the next year Selected papers from that workshop were published as the first volume of this series 21 The Computer Engineering Handbook Vojin G. Oklobdzija,2001-12-26

There is arguably no field in greater need of a comprehensive handbook than computer engineering The unparalleled rate of technological advancement the explosion of computer applications and the now in progress migration to a wireless world have made it difficult for engineers to keep up with all the developments in specialties outside their own **Defect and Fault Tolerance in VLSI Systems** Israel Koren,2012-12-06 This book contains an edited selection of papers presented at the International Workshop on Defect and Fault Tolerance in VLSI Systems held October 6 7 1988 in Springfield Massachusetts Our thanks go to all the contributors and especially the members of the program committee for the difficult and time consuming work involved in selecting the papers that were presented in the workshop and reviewing the papers included in this book Thanks are also due to the IEEE Computer Society in particular the Technical Committee on Fault Tolerant Computing and the Technical Committee on VLSI and the University of Massachusetts at Amherst for sponsoring the workshop and to the National Science Foundation for supporting under grant number MIP 8803418 the keynote address and the distribution of this book to all workshop attendees The objective of the workshop was to bring together researchers and practitioners from both industry and academia in the field of defect tolerance and yield enhancement in VLSI to discuss their mutual interests in defect tolerant architectures and models for integrated circuit defects faults and yield Progress in this area was slowed down by the proprietary nature of yield related data and by the lack of appropriate forums for disseminating such information The goal of this workshop was therefore to provide a forum for a dialogue and exchange of views A follow up workshop in October 1989 with C H Stapper from IBM and V K Jain from the University of South Florida as general co chairmen is being organized Manufacturing Yield Evaluation of VLSI/WSI Systems Bruno Ciciani,1995 A practical understanding of these concepts and their application can help to reduce the chance of having device failures

Proceedings of the ... Custom Integrated Circuits Conference ,1987 *Fault-Tolerant Systems* Israel Koren,C. Mani Krishna,2020-09-01 Fault Tolerant Systems Second Edition is the first book on fault tolerance design utilizing a systems

approach to both hardware and software No other text takes this approach or offers the comprehensive and up to date treatment that Koren and Krishna provide The book comprehensively covers the design of fault tolerant hardware and software use of fault tolerance techniques to improve manufacturing yields and design and analysis of networks Incorporating case studies that highlight more than ten different computer systems with fault tolerance techniques implemented in their design the book includes critical material on methods to protect against threats to encryption subsystems used for security purposes The text s updated content will help students and practitioners in electrical and computer engineering and computer science learn how to design reliable computing systems and how to analyze fault tolerant computing systems Delivers the first book on fault tolerance design with a systems approach Offers comprehensive coverage of both hardware and software fault tolerance as well as information and time redundancy Features fully updated content plus new chapters on failure mechanisms and fault tolerance in cyber physical systems Provides a complete ancillary package including an on line solutions manual for instructors and PowerPoint slides

Selected Papers on Statistical Design of Integrated Circuits Andrzej J. Strojwas,1987 Statistical Approach to VLSI Stephen W. Director,W. Maly,1994 This volume is the first complete overview of VLSI design methods that use statistical techniques for dealing with the random phenomena that are inherent in all VLSI manufacturing processes VLSI design today cannot be performed without taking into account economic related issues such as yield cost and performance oriented tradeoffs The book includes practical methods relevant to real life applications It contains edited papers by top industrial and academic specialists in the field These papers describe all three categories of CAD tools employed for statistical design IC performance optimization tools process simulation tools and tools for characterization of process fluctuations In each category both practical approaches and more theoretical approaches are presented The 17th Yugoslav Conference on Microelectronics: Proceedings N. Stojadinović,1989 **Proceedings, the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems, November 13-15, 1995, Lafayette, Louisiana** IEEE Computer Society,1995 An invited talk recounts Intel s experience with increasing die yield through CAD algorithms and a panel discussion examines tools for the extracting of critical areas for a yield analysis of VLSI design Others of the 34 papers cover critical area analysis defect sensitivity and reliability fault tolerant architectures and arrays yield projection and enhancement fault tolerant and testing techniques and self checking and coding techniques No subject index Annotation copyright by Book News Inc Portland OR **1986 Proceedings** Harold S. Stone,1986 *Proceedings of the IEEE 1987 Custom Integrated Circuits Conference* ,1987 **1986 Proceedings** IEEE Computer Society,1986 **IBM Journal of Research and Development** ,1989 *Yield and Variability Optimization of Integrated Circuits* Jian Cheng Zhang,M.A. Styblinski,2013-03-09 Traditionally Computer Aided Design CAD tools have been used to create the nominal design of an integrated circuit IC such that the circuit nominal response meets the desired performance specifications In reality however due to the disturbances ofthe IC manufacturing

process the actual performances of the mass produced chips are different than those for the nominal design. Even if the manufacturing process were tightly controlled so that there were little variations across the chips manufactured, the environmental changes e.g. those of temperature, supply voltages etc. would also make the circuit performances vary during the circuit life span. Process related performance variations may lead to low manufacturing yield and unacceptable product quality. For these reasons, statistical circuit design techniques are required to design the circuit parameters taking the statistical process variations into account. This book deals with some theoretical and practical aspects of IC statistical design and emphasizes how they differ from those for discrete circuits. It describes a spectrum of different statistical design problems such as parametric yield optimization, generalized on target design, variability minimization, performance tuning and worst case design. The main emphasis of the presentation is placed on the principles and practical solutions for performance variability minimization. It is hoped that the book may serve as an introductory reference material for various groups of IC designers and the methodologies described will help them enhance the circuit quality and manufacturability. The book contains seven chapters.

IEEE VLSI Test Symposium, 1999 **Integration of Test with Design and Manufacturing** IEEE Computer Society, 1987

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