



Thermal Testing Of Integrated Circuits

N Colangelo



Thermal Testing Of Integrated Circuits:

Thermal Testing of Integrated Circuits J. Altet, Antonio Rubio, 2013-03-09 Integrated circuits IC s have undergone a significant evolution in terms of complexity and performance as a result of the substantial advances made in manufacturing technology Circuits in their various mixed formats can be made up tens or even hundreds of millions of devices They work at extremely low voltages and switch at very high frequencies Testing of circuits has become an essential process in IC manufacturing in the effort to ensure that the manufactured components have the appropriate levels of quality Along with the ongoing trend towards more advanced technology and circuit features major testing challenges are continuously emerging The use of ambivalent procedures to test the analogue and digital sections of such complex circuits without interfering in their nominal operation is clearly a critical part of today s technological industries Chapter 1 presents the general purposes and basic concepts related With the testing of integrated circuits discussing the various strategies and their limitations Readers who are already familiar with the field may opt to skip this chapter This book offers a multidisciplinary focus on thermal testing This is a testing method which is not only suitable for use in combination with other existing techniques but is also backed by a wealth of knowledge and offers exciting opportunities in the form of as yet unexplored areas of research and innovation for industrial applications

Multi-scale Thermal and Circuit Analysis for Nanometre-scale Integrated Circuits Nicholas Allec, 2008 Chip temperature is increasing with continued technology scaling due to increased power density and decreased device feature sizes Since temperature has significant impact on performance and reliability accurate thermal and circuit analysis are of great importance Due to the shrinking device feature size effects occurring at the nanometre scale such as ballistic transport of energy carriers and electron tunneling have become increasingly important and must be considered However many existing thermal and circuit analysis methods are not able to consider these effects efficiently if at all This thesis presents methods for accurate and efficient multi scale thermal and circuit analysis For circuit analysis the simulation of single electron device circuits is specifically studied To target thermal analysis in this work ThermalScope a multi scale thermal analysis method for nanometre scale IC design is developed It unifies microscopic and macroscopic thermal physics modeling methods i e the Boltzmann transport and Fourier modeling methods Moreover it supports adaptive multi resolution modeling Together these ideas enable efficient and accurate characterization of nanometre scale heat transport as well as chip package level heat flow ThermalScope is designed for full chip thermal analysis of billion transistor nanometre scale IC designs with accuracy at the scale of individual devices ThermalScope has been implemented in software and used for full chip thermal analysis and temperature dependent leakage analysis of an IC design with more than 150 million transistors To target circuit analysis in this work SEMSIM a multi scale single electron device simulator is developed with an adaptive simulation technique based on the Monte Carlo method This technique significantly improves the time efficiency while maintaining accuracy for single electron device and circuit simulation It is

shown that it is possible to reduce simulation time up to nearly 40 times and maintain an average propagation delay error of under 5% compared to a non adaptive Monte Carlo method This simulator has been used to handle large circuit benchmarks with more than 6000 junctions showing efficiency comparable to SPICE with much better accuracy In addition the simulator can characterize important secondary effects including cotunneling and Cooper pair tunneling which are critical for device research

Annual IEEE Semiconductor Thermal Measurement and Management Symposium, 2005 *Design, Test and Certification Issues for Complex Integrated Circuits* L. Harrison, 1996 *Thermal Issues in Testing of Advanced Systems on Chip* Nima Aghaee Ghalesahi, 2015-09-23

Many cutting edge computer and electronic products are powered by advanced Systems on Chip SoC Advanced SoCs encompass superb performance together with large number of functions This is achieved by efficient integration of huge number of transistors Such very large scale integration is enabled by a core based design paradigm as well as deep submicron and 3D stacked IC technologies These technologies are susceptible to reliability and testing complications caused by thermal issues Three crucial thermal issues related to temperature variations temperature gradients and temperature cycling are addressed in this thesis Existing test scheduling techniques rely on temperature simulations to generate schedules that meet thermal constraints such as overheating prevention The difference between the simulated temperatures and the actual temperatures is called temperature error This error for past technologies is negligible However advanced SoCs experience large errors due to large process variations Such large errors have costly consequences such as overheating and must be taken care of This thesis presents an adaptive approach to generate test schedules that handle such temperature errors Advanced SoCs manufactured as 3D stacked ICs experience large temperature gradients Temperature gradients accelerate certain early life defect mechanisms These mechanisms can be artificially accelerated using gradient based burn in like operations so that the defects are detected before shipping Moreover temperature gradients exacerbate some delay related defects In order to detect such defects testing must be performed when appropriate temperature gradients are enforced A schedule based technique that enforces the temperature gradients for burn in like operations is proposed in this thesis This technique is further developed to support testing for delay related defects while appropriate gradients are enforced The last thermal issue addressed by this thesis is related to temperature cycling Temperature cycling test procedures are usually applied to safety critical applications to detect cycling related early life failures Such failures affect advanced SoCs particularly through silicon via structures in 3D stacked ICs An efficient schedule based cycling test technique that combines cycling acceleration with testing is proposed in this thesis The proposed technique fits into existing 3D testing procedures and does not require temperature chambers Therefore the overall cycling acceleration and testing cost can be drastically reduced All the proposed techniques have been implemented and evaluated with extensive experiments based on ITC 02 benchmarks as well as a number of 3D stacked ICs Experiments show that the proposed techniques work effectively and reduce the costs in particular the costs related to addressing thermal

issues and early life failures We have also developed a fast temperature simulation technique based on a closed form solution for the temperature equations Experiments demonstrate that the proposed simulation technique reduces the schedule generation time by more than half *Proceedings* ,1995 Linear Integrated Circuits and MOS Devices: Selection guide, data RCA Corporation. Solid State Division,1974 IEEE VLSI Test Symposium ,2004 **Proceedings of the ... International Symposium on Microelectronics** ,2000 **COS/MOS Digital Integrated Circuits** RCA Corporation. Solid State Division,1974 Thermal and Power Management of Integrated Circuits Arman Vassighi,Manoj Sachdev,2006-06-01 In Thermal and Power Management of Integrated Circuits power and thermal management issues in integrated circuits during normal operating conditions and stress operating conditions are addressed Thermal management in VLSI circuits is becoming an integral part of the design test and manufacturing Proper thermal management is the key to achieve high performance quality and reliability Performance and reliability of integrated circuits are strong functions of the junction temperature A small increase in junction temperature may result in significant reduction in the device lifetime This book reviews the significance of the junction temperature as a reliability measure under nominal and burn in conditions The latest research in the area of electro thermal modeling of integrated circuits will also be presented Recent models and associated CAD tools are covered and various techniques at the circuit and system levels are reviewed Subsequently the authors provide an insight into the concept of thermal runaway and how it may best be avoided A section on low temperature operation of integrated circuits concludes the book *Linear Integrated Circuits and MOS Devices* RCA Corporation. Solid State Division,1973 Linear Integrated Circuits and MOS Devices: Application notes RCA Corporation. Solid State Division,1974 **Government Reports Announcements & Index** ,1988 **16th Annual GaAs IC Symposium** ,1994 **An Introductory Guide to EC Competition Law and Practice** Valentine Korah,1994 **1996 International Symposium on Microelectronics** ,1996 **Proceedings of the National Communications Forum** ,1967 Thirteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium Institute of Electrical and Electronics Engineers,1997 This volume features coverage of new developments in and applications relating to generation and removal of heat within semiconductor devices and measurement of junction temperatures under various application and environmental conditions **Handbook of 3D Integration, Volume 4** Paul D. Franzon,Erik Jan Marinissen,Muhannad S. Bakir,2019-01-25 This fourth volume of the landmark handbook focuses on the design testing and thermal management of 3D integrated circuits both from a technological and materials science perspective Edited and authored by key contributors from top research institutions and high tech companies the first part of the book provides an overview of the latest developments in 3D chip design including challenges and opportunities The second part focuses on the test methods used to assess the quality and reliability of the 3D integrated circuits while the third and final part deals with thermal management and advanced cooling technologies and their integration

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