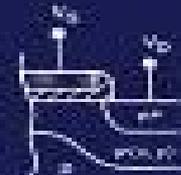
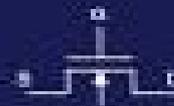


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COMPUTER SIMULATION OF IC PROCESSES AND DEVICES



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Tomacruz,1994 **Computer-aided Design of Microelectronic Circuits and Systems: General introduction and analog-circuit aspects** A. F. Schwarz,1987 IEEE Circuits & Devices ,2001 Proceedings of the ... International Symposium on Power Semiconductor Devices and ICs ,1992 **Digital Timing Macromodeling for VLSI Design Verification** Jeong-Taek Kong,David V. Overhauser,1995-05-31 Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques It presents detailed discussion of the various techniques implemented in circuit timing fast timing switch level timing switch level and gate level simulation It also discusses mixed mode simulation and interconnection analysis methods The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels Specifically the techniques address the device model detail transistor coupling capacitance effective channel length modulation series transistor reduction effective transconductance input terminal dependence gate parasitic capacitance the body effect the impact of parasitic RC interconnects and the effect of transmission gates The techniques address major sources of errors in existing macromodeling techniques which must be addressed if macromodeling is to be accepted in commercial CAD tools by chip designers The techniques presented in Chapters 4 6 can be implemented in other macromodels and are demonstrated using the macromodel presented in Chapter 3 The new techniques are validated over an extremely wide range of operating conditions much wider than has been presented for previous macromodels thus demonstrating the wide range of applicability of these techniques **SIMPL-2 (simulated Profiles from the Layout - Version 2)** Keunmyung Lee,1985 Formal Semantics for VHDL Carlos Delgado Kloos,P. Breuer,1995-02-28 Research papers from a January 1994 workshop put forth a cohesive set of semantics for the VHDL language and describe semantics based on Petri nets as target language higher order logic functional concepts and evolving algebras Quotes from Lewis Carroll s Alice Through the Looking Glass introduce each paper For researchers in formal methods and advanced students No index Annotation copyright by Book News Inc Portland OR *Process Compilation Methods for Thin Film Devices* Mohammed Hasanuz Zaman,1997 *Simulation of Semiconductor Devices and Processes, Vol. 3* Giorgio Baccarani,Massimo Rudan,1988 Asymptotic Waveform Evaluation Eli Chiprout,Michel S. Nakhla,1994 The intense drive for signal integrity has been at the forefront of rapid and new developments in CAD algorithms With increasing demands for high signal speeds coupled with a decrease in feature size interconnect effects such as signal delay distortion and crosstalk become the dominant factor limiting overall performance of VLSI systems Although SPICE is used on a daily basis by many engineers for analog simulation and general circuit analysis current versions of SPICE do not handle adequately the new emerging challenges of interconnect effects Moment matching techniques such as asymptotic waveform evaluation have recently proven useful in the analysis of large interconnect structures containing elements such as lossy

coupled transmission lines with linear or nonlinear terminations At a CPU cost of a little more than one DC analysis these techniques are 2-3 orders of magnitude faster than full simulation techniques such as FFT Asymptotic Waveform Evaluation presents an overview of the diverse algorithms and applications of moment matching techniques The material is presented systematically and is supported by many examples Issues such as sensitivity analysis and three dimensional analysis are also covered Asymptotic Waveform Evaluation will be of interest to engineers students and researchers involved in the development and study of circuit simulation as well as interconnect analysis It will also interest design engineers who are involved in dealing with high speed issues and graduate students who are active in the development of CAD tools for electronic systems

Process and Device Modeling for Integrated Circuit Design F. van de Wiele, W.L. Engl, P. Jespers, 1977-11-30 An Advanced Study Institute on process and device modeling for integrated circuit design was held in Louvain la Neuve Belgium on July 19-29 1977 under the auspices of the Scientific Affairs Division of NATO The Institute was organized by a scientific organizing committee consisting of Professor F Van de Wiele of the Universite Catholique de Louvain Professor W L Engl of the Technische Hochschule Aachen and Professor P Jespers of the Universite Catholique de Louvain This book represents the contributions of the lecturers at the Institute and the chapters present a concise treatment of a very timely subject namely process and device modeling for integrated circuit design The organization of the book parallels the program at the Institute with an introduction comprised of a review of modeling and basic semiconductor physics This is followed by the chapters devoted to basic technologies modeling of bipolar and MoS devices The last chapter of the book presents the specific topic of process modeling The subject matter of this book is suitable for a wide range of interests from the advanced student through the practicing physicist and engineer to the research worker Although a novice may find some difficulty with the mathematical development he can acquire a perspective into the field of process and device modeling for integrated circuit design with this book Likewise portions of this book may be used as a textbook since the chapters are instructional and self contained

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