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Kiyoo Itoh

VLSI Memory Chip Design



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Jin-Ying Zhang



Vlsi Memory Chip Design:

VLSI Memory Chip Design Kiyoo Itoh, 2013-04-17 The VLSI memory era truly began when the first production of semiconductor memory was announced by IBM and Intel in 1970. The announcement had a profound impact on my research at Hitachi Ltd and I was forced to change fields from magnetic thin film to semiconductor memory. This change was so exceptionally sudden and difficult I felt like a victim of fate. Looking back however I realize how fortunate I was. I have witnessed an unprecedented increase in memory capacity. DRAM for example has had a 6 order increase in the last three decades from the 1 Kb level in 1970 to the 1 Gb level today. I have contributed to this progress with full involvement in memory chip development over my career. Such rapid progress would have been impossible without many of the inventions and innovative technologies and without the effort of many talented people. Unfortunately few systematic books on memory chip design have been written by experts. This is a result of two factors: the difficulty of involving university professors because of rapidly changing technology requiring huge investments and development resources and a shortage of time on the part of chip designers in industry due to severe competition in the memory chip business. Therefore LSI memory chip design has been isolated from the outside preventing a deeper understanding of the technology. This book is based on my 30 year memory chip particularly DRAM design career.

Vlsi Memory Chip Design Itoh, 2006-06-01 *Nanoscale Memory Repair* Masashi Horiguchi, Kiyoo Itoh, 2011-01-11 Yield and reliability of memories have degraded with device and voltage scaling in the nano scale era due to ever increasing hard soft errors and device parameter variations. This book systematically describes these yield and reliability issues in terms of mathematics and engineering as well as an array of repair techniques based on the authors long careers in developing memories and low voltage CMOS circuits. *Nanoscale Memory Repair* gives a detailed explanation of the various yield models and calculations as well as various practical logic and circuits that are critical for higher yield and reliability.

IEEE VLSI Test Symposium, 1990 **VLSI System Test**, 1990 Proceedings, Conference on Advanced Research in VLSI Paul Penfield, 1981 **Integrated Circuit Design**, 2002 *Proceedings*, 2002

Design Methodology for Three-dimensional CMOS Integrated Circuits Branislav Jovan Vajdic, 1984 *Proceedings of the 12th Conference on Solid State Devices, Tokyo, 1980*, 1981 *Report*, 1987 **The Chipmakers** Time-Life Books, 1990 The Israel Economist, 1986 **Advances in Powder Technology** Gilbert Y. Chin, American Society for Metals. Materials Science Division, 1982 *Computer Design*, 1982 Digest of Technical Papers International Conference on Computer-Aided Design, 1984 *Proceedings of the ISMM International Conference* Z. Jacyno, 1990

Scaling CMOS Memories Charles C. Kuo, 2002 **IEICE Transactions on Electronics**, 2007 *International Workshop on Memory Technology, Design, and Testing* Fabrizio Lombardi, Rochit Rajsuman, Thomas Wik, 2001 Annotation The 14 papers in this collection from the August 2001 workshop are divided into five sessions on semiconductor memory design BIST redundancy and error control fault models and multi port SRAM testing and verification and testing Some of the

topics are evaluation of redundancy analysis algorithms a parallel approach for testing multi port static random access memories a low output resistance charge pump for flash memory programming BIST based bitfail mapping of an embedded DRAM and an orthogonal transpose RAM cell array architecture with an alternate bit line to bit line contact scheme No subject index c Book News Inc

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