VLSI Architecture

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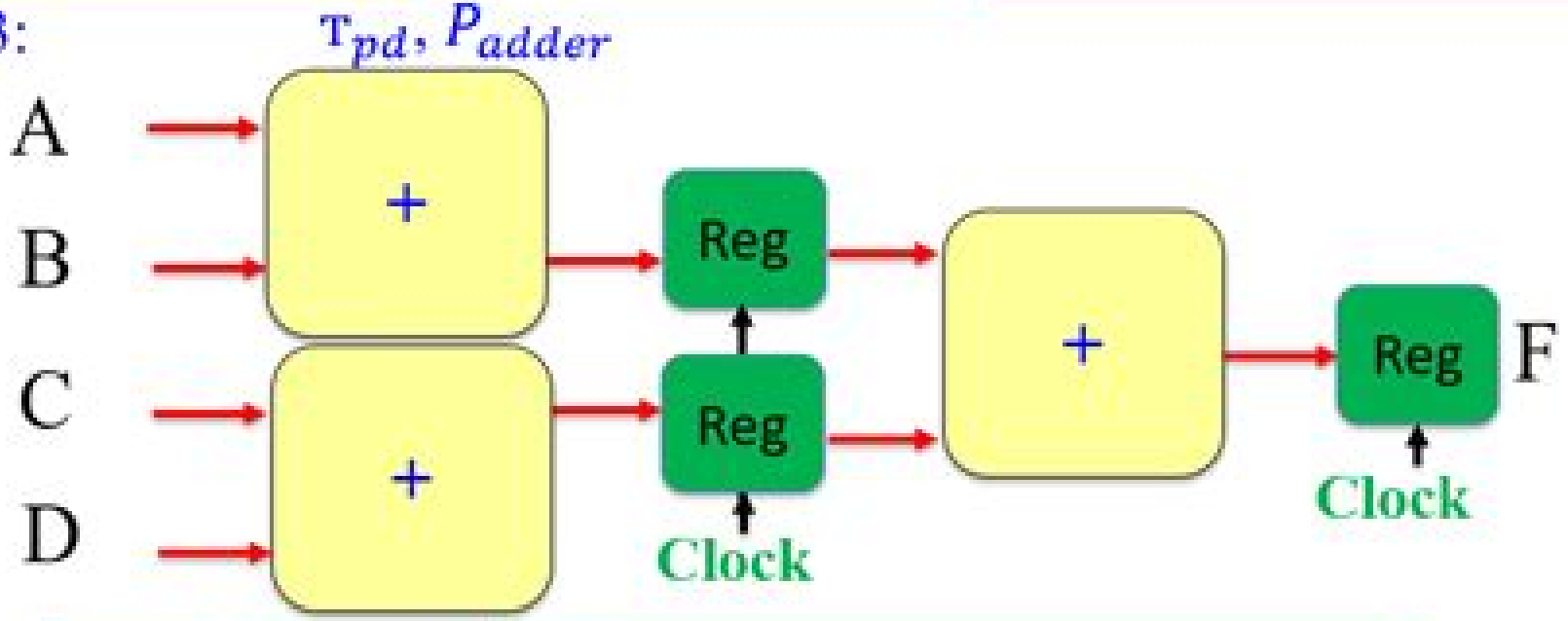

Performance Figure	Value
Function Delay	$2^{*}T_{Clock}$
Power	$3 * P_{adder} + 3 * P_{Regsiter}$
Throughput	@ T_{Clock} ($T_{clk-Q} + T_{pd_adder} + T_{setup}$)
Gate complexity	$3 * G_{adder} + 2 * G_{Register}$
Functional Flexibility	Nil
Function Expandability	Nil

Vlsi Architecture

Daniel D. Gajski

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