
Switch-Level Timing Simulation of MOS VLSI Circuits

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Switchlevel Timing Simulation Of Mos Vlsi Circuits

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Switchlevel Timing Simulation Of Mos Vlsi Circuits:

Switch-Level Timing Simulation of MOS VLSI Circuits Vasant B. Rao, David V. Overhauser, Timothy N. Trick, Ibrahim N. Hajj, 2012-12-06 Only two decades ago most electronic circuits were designed with a slide rule and the designs were verified using breadboard techniques. Simulation tools were a research curiosity and in general were mistrusted by most designers and test engineers. In those days the programs were not user friendly, models were inadequate and the algorithms were not very robust. The demand for simulation tools has been driven by the increasing complexity of integrated circuits and systems and it has been aided by the rapid decrease in the cost of computing that has occurred over the past several decades. Today a wide range of tools exist for analysis, design and verification and expert systems and synthesis tools are rapidly emerging. In this book only one aspect of the analysis and design process is examined but it is a very important aspect that has received much attention over the years. It is the problem of accurate circuit and timing simulation.

Switch-level Timing Simulation of MOS VLSI Circuits Vasant Bangalore Rao, 1985 This report deals with the development of a fast and accurate simulation tool for very large scale integrated VLSI circuits consisting of metal oxide semiconductor MOS transistors. Such tools are called switch level timing simulators and they provide adequate information on the performance of the circuits with a reasonable expenditure of computation time even for very large circuits. The algorithms presented in this thesis can handle only n channel MOS NMOS circuits but are easily extendible to handle complementary MOS CMOS circuits as well. The algorithms presented in this report have been implemented in a computer program called MOSTIM. In all the circuits simulated thus far MOSTIM provides timing information with an accuracy of within 10% of that provided by SPICE2 at approximately two orders of magnitude faster in simulation speed. Author

Switch-Level Timing Simulation of MOS VLSI (Metal-Oxide-Semiconductor Very Large-Scale Integrated) Circuits Vasant B. Rao, ILLINOIS UNIV AT URBANA COORDINATED SCIENCE LAB., 1985 This report deals with the development of a fast and accurate simulation tool for very large scale integrated VLSI circuits consisting of metal oxide semiconductor MOS transistors. Such tools are called switch level timing simulators and they provide adequate information on the performance of the circuits with a reasonable expenditure of computation time even for very large circuits. The algorithms presented in this thesis can handle only n channel MOS NMOS circuits but are easily extendible to handle complementary MOS CMOS circuits as well. The algorithms presented in this report have been implemented in a computer program called MOSTIM. In all the circuits simulated thus far MOSTIM provides timing information with an accuracy of within 10% of that provided by SPICE2 at approximately two orders of magnitude faster in simulation speed. Author

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Systems serves as an excellent reference providing insight into some of the most challenging research issues in the field

Digital Timing Macromodeling for VLSI Design Verification Jeong-Taek Kong, David V. Overhauser, 2012-12-06

Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques It presents detailed discussion of the various techniques implemented in circuit timing fast timing switch level timing switch level and gate level simulation It also discusses mixed mode simulation and interconnection analysis methods The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels Specifically the techniques address the device model detail transistor coupling capacitance effective channel length modulation series transistor reduction effective transconductance input terminal dependence gate parasitic capacitance the body effect the impact of parasitic RC interconnects and the effect of transmission gates The techniques address major sources of errors in existing macromodeling techniques which must be addressed if macromodeling is to be accepted in commercial CAD tools by chip designers The techniques presented in Chapters 4 6 can be implemented in other macromodels and are demonstrated using the macromodel presented in Chapter 3 The new techniques are validated over an extremely wide range of operating conditions much wider than has been presented for previous macromodels thus demonstrating the wide range of applicability of these techniques

Micro System Technologies 90 Herbert Reichl, 2012-12-06 On September 10 13 1990 the first international meeting on Microsystem Technologies takes place at the Berlin International Congress Center Most of the traditional congresses deal with themes that become more and more specific and only a small part of the scientific world is reflected The Micro System Technologies is attempting to take the opposite direction During the last two decades the development of microelectronics was characterized by a tremendous increase of complexity of integrated circuits At the same time the fields of microoptics and micromechanics have been developed to an advanced state of the art by the application of thin film and semiconductor technologies The trend of the future development is to increase the integration density by combining the microelectronic microoptic and micro mechanic aspects to new complex multifunctional systems which are able to comprise sensors actuators analogue and digital circuits on the same chip or on multichip modules Microsystems will lead to extensions of the field of microelectronic applications with important technical alterations and can open new considerable markets For the realization of economical solutions for microsystems a lot of interdisciplinary cooperation and know how has to be developed New materials for sensitive layers substrates conducting semiconducting or isolating thin films are the basis for the development of new technologies The increasing complexity leads to increasing interaction among electrical and non electrical quantities

1991 IEEE International Symposium on Circuits and Systems, 1991 **1987 IEEE Workshop on Languages for Automation**

,1987 *Circuit Analysis, Simulation and Design* Albert E. Ruehli,1987 This book covers algorithmic aspects of computer aided circuit design for VLSI of large circuits The large scale aspect of VLSI requires a reorientation towards new and more efficient techniques Many algorithms have survived the test of time while others are suffering from the usual problem of polynomial or exponential running time complexity and storage requirements The approaches presented in this book are techniques which were developed in response to the VLSI problems The most recent exact circuit analysis and simulation techniques are presented such as waveform relaxation and timing simulation The book concentrates on the analysis and simulation of large circuits which exceed the capabilities of general purpose analyzers in both compute time and storage Also discussed are circuit models for switch level simulation techniques and circuit models for interconnections capacitance and inductances and optimization techniques The language and notation have been kept uniform throughout the book to help the reader to maintain the continuity between the topics discussed in the different chapters All algorithms are written in a Pascal style The terminology used should reflect the emerging language used in most of the VLSI circuit design community The book includes proven approaches as well as techniques which are presently in a research state **IEEE International Symposium on Circuits and Systems** ,1988 1993 International Symposium on VLSI Technology, Systems, and Applications ,1993 Digital Timing Macromodeling for VLSI Design Verification Jeong-Taek Kong,David V. Overhauser,1995-05-31 Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques It presents detailed discussion of the various techniques implemented in circuit timing fast timing switch level timing switch level and gate level simulation It also discusses mixed mode simulation and interconnection analysis methods The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels Specifically the techniques address the device model detail transistor coupling capacitance effective channel length modulation series transistor reduction effective transconductance input terminal dependence gate parasitic capacitance the body effect the impact of parasitic RC interconnects and the effect of transmission gates The techniques address major sources of errors in existing macromodeling techniques which must be addressed if macromodeling is to be accepted in commercial CAD tools by chip designers The techniques presented in Chapters 4 6 can be implemented in other macromodels and are demonstrated using the macromodel presented in Chapter 3 The new techniques are validated over an extremely wide range of operating conditions much wider than has been presented for previous macromodels thus demonstrating the wide range of applicability of these techniques *1995 International Symposium on VLSI Technology, Systems, and Applications* ,1995 *IEEE Circuits & Devices* ,1995 **Digest of Technical Papers** ,1988 1987 IEEE International Symposium on Circuits and Systems ,1987 **Proceedings** ,1985

Progress in Computer-aided VLSI Design: Techniques George Winston Zobrist, 1990 These volumes review late 1980s early 1990s state of the art developments in computer aided design and analysis techniques Contributions from researchers and practitioners include discussions of parallel algorithms and fundamental operations in cryptography systolic arrays and pipelined designs 1995 IEEE TENCON Institute of Electrical and Electronics Engineers. Region 10. Conference on Microelectronics and VLSI, 1995

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