A Constructive Approach for Threshold Logic Circuit Synthesis

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Abstract – In this paper, a novel method to synthesize circuits based on threshold logic gates (TLG) is proposed. Synthesis considering TLGs is quite relevant, since threshold logic has been revisited as a promising alternative to conventional CMOS integrated circuits due to its suitability to emerging technologies, such as tunneling diodes, memristors and spintronics devices. A constructive process is applied to generate optimized TLG networks taking into account multiple goals and design costs, including gate count, logic depth and number of interconnections. Experiments carried out over MCNC benchmark circuits have shown an average gate count reduction of circa 32%, reaching up to 54% in some cases, in comparison to related approaches.

Keywords – Digital circuit, logic synthesis, threshold logic, functional composition, threshold networks, TLG.

I. INTRODUCTION

The limits of MOS transistor scaling have motivated investigations about new alternative devices, such as spintronics, resonant tunneling devices (RTD), quantum cellular automata (QCA), single electron transistor (SET) and memristors [1]-[3]. In this new scenario, it has been verified that threshold logic gates (TLG) are more suitable to implement digital integrated circuits (ICs) based on these new technologies, differently from the standard AND/OR based CMOS circuit design [4][5].

However, specific CAD tools must be available for developing TLG based ICs. In this sense, one critical task is to obtain efficient network built using TLGs to implement a specific Boolean function. In [5], Zhang *et al.* proposed a recursive partition of a logic function that is not threshold and merge nodes respecting fan-in restrictions. Unfortunately, the quality of results is very sensitive to the initial Boolean network. On the other hand, the method presented by Subirats *et al.*, in [6], is based on the truth table description of the function. The algorithm compute an ordering of variables using information of on-set and off-set, performing Shannon decomposition up to find threshold logic functions (TLF). However, this approach provides as output a two-level threshold network, without fan-in restriction, being more suitable for neural networks than for IC design. In [7], Gowda *et al.* used a factorized tree to generate a network of threshold gates. The method recursively breaks the given initial expression tree into sub-expressions, identifying sub-tree that are TLFs and assigning the input weights. It is appropriate for IC synthesis using several TLGs, but represents a very time consuming process and presents a strong dependence to the initial expression structure, including the ordering of the initial tree.

In this paper, an algorithm is proposed to synthesize threshold networks aiming to (1) minimize threshold networks taking into account other costs besides threshold gate count, like logic depth and number of interconnections, (2) generate more than one effective solution, considering a design cost order, and (3) eliminate the structural bias dependence in order to improve the quality of results. It is based on a constructive synthesis [8]-[10], which associates simpler sub-solutions with known costs in order to build more complex networks, allowing the optimization of different cost functions other than just the TLG count. The algorithm uses a novel AND/OR association between threshold networks to reduce the total number of TLGs in the circuit.

The rest of this paper is organized as follows. In Section II, some fundamentals are briefly presented for a better understanding of our approach. Section III describes the algorithm proposed to synthesize threshold logic networks. Section IV provides the experimental results, whereas the conclusions are outlined in Section V.

II. PRELIMINARIES

First of all, basic concepts of threshold logic are briefly reviewed for a better understanding of the proposed method.

A. Threshold Logic Gate

Differently from the traditional logic gate design, the threshold logic gate (TLG) implements Boolean function considering weight values for inputs (function variables) and a gate threshold value to be attained. If the sum of weights of activate ('1') inputs is equal to or higher than the given threshold value, then the output logic level of the TLG is high ('1'). Otherwise, the gate output is at low level ('0'). Such operating principle can be expressed as follows:

$$f = \begin{cases} 1 & g \sum_{i=1}^{n} w_i x_i \geq T \\ 0 & ,otherwise \end{cases} \quad (1)$$

where x_i and w_i represent the logic value and weight of each input, respectively, and T is the threshold value [11].

B. Threshold Logic Function

Threshold logic function (TLF), also called linearly separable function, is a Boolean function that can be implemented into a single TLG. TLF can be completely represented in a compact vector format such as $[w_1, w_2, ..., w_n; T]$. For instance, the function $f = x_1 x_2 + x_3 x_4$ can be represented as $f = [2,1,1;3]$.

Threshold Logic A Synthesis Approach

Stanley Leonard Hurst

Threshold Logic A Synthesis Approach:

Threshold Logic Michael L. Dertouzos,1965   *Synthesis and Testing of Threshold Logic Circuits* Ashok Kumar Palaniswamy,2014 Threshold logic gates gaining more importance in recent years due to the significant development in the switching devices This renewed the interest in synthesis and testing of circuits with threshold logic gates Two important synthesis considerations of threshold logic circuits are addressed namely threshold logic function identification and reducing the total number of threshold logic gates required to represent the given boolean circuit description A fast method to identify the given Boolean function as a threshold logic function with weight assignment is introduced It characterizes the threshold logic function based on the modified chows parameters which results in drastic reduction in time and complexity Experiment results shown that the proposed method is at least 10 times faster for each input and around 20 times faster for 7 and 8 input when comparing with the algorithmic based methods Similarly it is 100 times faster for 8 input when comparing with asummable method Existing threshold logic synthesis methods decompose the larger input functions into smaller input functions and perform synthesis for them This results in increase in the number of threshold logic gates required to represent the given circuit description The proposed implicit synthesis methods increase the size of the functions that can be handled by the synthesis algorithm thus the number of threshold logic gates required to implement very large input function decreases Experiment results shown that the reduction in the TLG count is 24% in the best case and 18% on average An automatic test pattern generation approach for transition faults on a circuit consisting of current mode threshold logic gates is introduced The generated pattern for each fault excites the maximum propagation delay at the gate the fault site This is a high quality ATPG Since current mode threshold logic gate circuits are pipelined and the combinational depth at each pipeline stage is practically one It is experimentally shown that the fault coverage for all benchmark circuits is approximately 97% It is also shown that the proposed method is time efficient   *Switching and Finite Automata Theory* Zvi Kohavi,Niraj K. Jha,2010 Understand the structure behavior and limitations of logic machines with this thoroughly updated third edition Many new topics are included such as CMOS gates logic synthesis logic design for emerging nanotechnologies digital system testing and asynchronous circuit design to bring students up to speed with modern developments The intuitive examples and minimal formalism of the previous edition are retained giving students a text that is logical and easy to follow yet rigorous Kohavi and Jha begin with the basics and then cover combinational logic design and testing before moving on to more advanced topics in finite state machine design and testing Theory is made easier to understand with 200 illustrative examples and students can test their understanding with over 350 end of chapter review questions   **Applied Automata Theory** Julius T. Tou,2013-10-22 Applied Automata Theory provides an engineering style of presentation of some of the applied work in the field of automata theory Topics covered range from algebraic foundations and recursive functions to regular expressions threshold logic and switching circuits Coding problems and stochastic processes are also discussed along with

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