

Harmony: Static Noise Analysis of Deep Submicron Digital Integrated Circuits

Kenneth L. Shepard, Member, IEEE, Vinod Narayanan, Senior Member, IEEE, and Ron Rose

Abstract—As technology scales into the deep submicron regime, noise immunity is becoming a metric of comparable importance to area, timing, and power for the analysis and design of very large scale integrated (VLSI) systems. A metric for noise immunity is defined, and a static noise analysis methodology based on this noise-stability metric is introduced to demonstrate how noise can be analyzed systematically on a full-chip basis using simulation-based transistor-level analysis. We then describe Harmony, a two-level (macro and global) hierarchical implementation of static noise analysis. At the macro level, simplified interconnect models and timing assumptions guide efficient analysis. The global level involves a careful combination of static noise analysis, static timing analysis, and detailed interconnect macromodels based on reduced-order modeling techniques. We describe how the interconnect macromodels are practically employed to perform coupling analysis and how timing constraints can be used to limit pessimism in the analysis.

Index Terms—Deep-submicron IC's, interconnect coupling, signal integrity, static noise analysis.

I. INTRODUCTION

NOISE has traditionally been a concern to analog designers, since it represents a lower bound on the magnitude of a signal that can be usefully amplified. It also presents an upper bound to the useful gain of an amplifier, since noise will ultimately saturate an amplifier if the gain is too high. The noise sources of concern in analog design derive from physical sources—thermal noise, flicker noise, and shot noise, for example. These physical noise sources come about because of the discreteness of electronic charge and the stochastic nature of electronic transport processes [1].

In contrast, digital circuits, by virtue of the large, abrupt voltage swings characteristic of their operation, create deterministic man-made noise several orders of magnitude greater than noise from stochastic physical sources. Problems due to these noise sources were first observed in mixed-signal applications [2], [3], which plunged highly noise-sensitive analog circuits into a noisy digital environment. Although digital circuits create much more noise than analog circuits, digital systems are prevalent because they are inherently

immune to noise. Until recently, noise immunity overcame the noisiness of digital circuits. Technology scaling and performance demands have unfortunately changed this balance, and noise is now a problem even in purely digital designs.

Noise has become a metric in the design of digital integrated circuits of comparable importance to area, timing, and power for four principle reasons: increasing interconnect densities, faster clock rates, more aggressive use of high-performance circuit families, and scaling threshold voltages. All of these factors degrade the signal-to-noise ratio for CMOS digital designs. Increasing interconnect densities imply a significant increase in coupling capacitance as a fraction of self-capacitance. Faster clock rates imply faster on-chip slew times. These two effects combine to make capacitive coupling a growing source of noise on-chip. Many high-performance circuit styles try to speed up one transition (usually falling) at the expense of the other and assign logical evaluations to the faster edge. Any circuit that utilizes these techniques we refer to as a *skewed-evaluate* circuit. Skewed-evaluate circuits have noise sensitivities directly related to the threshold voltages of the transistors responsible for the evaluate transitions [usually n-channel field-effect transistors (n-FET's)]. Threshold voltages are, however, scaling lower to maintain drive in the presence of scaling supply voltages. These effects combine to produce more sources of on-chip noise due to switching circuits as well as less immunity to this noise. More details of these technology trends can be found in [4].

Noise has two deleterious effects on digital design. When noise acts against a normally static signal, it can transiently destroy the logical information carried by the static node in the circuit. If this ultimately results in incorrect machine state stored in a latch, functional failure will result. When noise acts simultaneously with a switching node, this is manifest as a change in the timing (delay and slew) of the transition (a noise-on-delay effect). We are concerned with the former effect in this paper.

We present the first comprehensive methodology for understanding and analyzing the noise immunity of digital integrated circuits. There are three essential components of this static noise analysis: calculating noise due to coupling in the interconnects, calculating noise injected or propagated by the circuits, and having a criterion for deciding when the noise occurring on a node due to circuit and interconnect noise exceeds the noise immunity of the receiving circuits. In Section II, we introduce a noise classification based on the noise level relative to the supply and ground rails. We also describe the noise sources that are affecting digital design

Manuscript received August 29, 1997; revised July 3, 1998. The work performed at Columbia University was supported in part by the National Science Foundation (NSF) under Grant CCR-97-34216. This paper was recommended by Associate Editor K. Mayaram.

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Publisher Item Identifier S 0278-0076(99)05683-3.

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