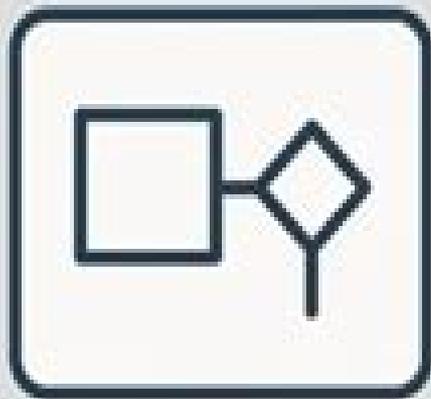


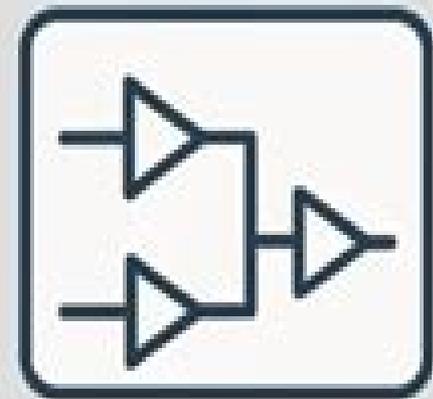
LOGIC SYNTHESIS IN VLSI



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INPUT**



**SYNTHESIS
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**GATE-LEVEL
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