



# That Girl From Happy

**Christian Drosten**



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web control of the i2c bus may be taken when the p bit is set or the bus is idle in firmware controlled master mode user

code conducts all i<sup>2</sup>c bus operations based on start and stop bit condition detection start and stop condition detection is  
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web bidirectional i<sup>2</sup>c stands for inter integrated circuit communications i<sup>2</sup>c is implemented in the picmicro by a hardware module called the master synchronous serial port known as the mssp module

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web c bus is a two wire serial bus with multiple possible masters and multiple possible slaves connected to each other through two wires the two wires consists of a clock line scl and a data line sda with both lines being bi directional

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web the master synchronous serial port mssp is an integrated serial communications module the mssp contains two sub modules spi serial peripheral interface i<sup>2</sup>c inter integrated circuit the inter integrated circuit commonly referred to as i<sup>2</sup>c is a synchronous two wire bidirectional serial communications bus

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web jun 23 2016 key features of the i<sup>2</sup>c module include the following independent master and slave logic multi master support which prevents message losses in arbitration detects 7 bit and 10 bit device addresses with configurable address masking in slave mode detects general call addresses as defined in the i<sup>2</sup>c protocol automatic sclx clock

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web the i<sup>2</sup>c bus is a multi master serial data communication bus microcontrollers communicate in a master slave environment where the master devices initiate the communication and the devices are selected through addressing i<sup>2</sup>c

operates with one or more master devices and one or more slave devices

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