

**VLSI Fault Modeling
and
Testing Techniques**

**edited by
George W. Zobrist**

Vlsi Fault Modeling And Testing Techniques

Constantin C. Timoc



Vlsi Fault Modeling And Testing Techniques:

VLSI Fault Modeling and Testing Techniques George W. Zobrist,1993 VLSI systems are becoming very complex and difficult to test Traditional stuck at fault problems may be inadequate to model possible manufacturing defects in the integrated circuit Hierarchical models are needed that are easy to use at the transistor and functional levels Stuck open faults present severe testing problems in CMOS circuits to overcome testing problems testable designs are utilized Bridging faults are important due to the shrinking geometry of ICs BIST PLA schemes have common features controllability and observability which are enhanced through additional logic and test points Certain circuit topologies are more easily testable than others The amount of reconvergent fan out is a critical factor in determining realistic measures for determining test generation difficulty Test implementation is usually left until after the VLSI data path has been synthesized into a structural description This leads to investigation methodologies for performing design synthesis with test incorporation These topics and more are discussed

Delay Fault Testing for VLSI Circuits Angela Krstic,Kwang-Ting (Tim) Cheng,1998-10-31 With the ever increasing speed of integrated circuits violations of the performance specifications are becoming a major factor affecting the product quality level The need for testing timing defects is further expected to grow with the current design trend of moving towards deep submicron devices After a long period of prevailing belief that high stuck at fault coverage is sufficient to guarantee high quality of shipped products the industry is now forced to rethink other types of testing Delay testing has been a topic of extensive research both in industry and in academia for more than a decade As a result several delay fault models and numerous testing methodologies have been proposed Delay Fault Testing for VLSI Circuits presents a selection of existing delay testing research results It combines introductory material with state of the art techniques that address some of the current problems in delay testing Delay Fault Testing for VLSI Circuits covers some basic topics such as fault modeling and test application schemes for detecting delay defects It also presents summaries and conclusions of several recent case studies and experiments related to delay testing A selection of delay testing issues and test techniques such as delay fault simulation test generation design for testability and synthesis for testability are also covered Delay Fault Testing for VLSI Circuits is intended for use by CAD and test engineers researchers tool developers and graduate students It requires a basic background in digital testing The book can be used as supplementary material for a graduate level course on VLSI testing

Introduction to Microelectronics to Nanoelectronics Manoj Kumar Majumder,Vijay Rao Kumbhare,Aditya Japa,Brajesh Kumar Kaushik,2020-11-24 Focussing on micro and nanoelectronics design and technology this book provides thorough analysis and demonstration starting from semiconductor devices to VLSI fabrication designing analog and digital on chip interconnect modeling culminating with emerging non silicon nano devices It gives detailed description of both theoretical as well as industry standard HSPICE Verilog Cadence simulation based real time modeling approach with focus on fabrication of bulk and nano devices Each chapter of this proposed title starts with a brief introduction of the presented

topic and ends with a summary indicating the futuristic aspect including practice questions Aimed at researchers and senior undergraduate graduate students in electrical and electronics engineering microelectronics nanoelectronics and nanotechnology this book Provides broad and comprehensive coverage from Microelectronics to Nanoelectronics including design in analog and digital electronics Includes HDL and VLSI design going into the nanoelectronics arena Discusses devices circuit analysis design methodology and real time simulation based on industry standard HSPICE tool Explores emerging devices such as FinFETs Tunnel FETs TFETs and CNTFETs including their circuit co designing Covers real time illustration using industry standard Verilog Cadence and Synopsys simulations

Realistic Fault Modeling for VLSI Testing Carnegie-Mellon University. SRC-CMU Research Center for Computer-Aided Design, W. Maly, 1987 Abstract Functional failures of VLSI circuits are caused by process induced defects Such defects have very complex physical characteristics and may be significantly different from the simplistic defect models assumed by typical fault modeling techniques In the tutorial an overview of the actual mechanisms causing processing defects and the defects electrical manifestations will be discussed It will be demonstrated that inadequate insight into the physics of processing defects and the manufacturing process may lead to inefficient testing of actual VLSI circuits

Hierarchical Modeling for VLSI Circuit Testing Debashis Bhattacharya, John P. Hayes, 2012-12-06 Test generation is one of the most difficult tasks facing the designer of complex VLSI based digital systems Much of this difficulty is attributable to the almost universal use in testing of low gate level circuit and fault models that predate integrated circuit technology It is long been recognized that the testing problem can be alleviated by the use of higher level methods in which multigate modules or cells are the primitive components in test generation however the development of such methods has proceeded very slowly To be acceptable high level approaches should be applicable to most types of digital circuits and should provide fault coverage comparable to that of traditional low level methods The fault coverage problem has perhaps been the most intractable due to continued reliance in the testing industry on the single stuck line SSL fault model which is tightly bound to the gate level of abstraction This monograph presents a novel approach to solving the foregoing problem It is based on the systematic use of multibit vectors rather than single bits to represent logic signals including fault signals A circuit is viewed as a collection of high level components such as adders multiplexers and registers interconnected by n bit buses To match this high level circuit model we introduce a high level bus fault that in effect replaces a large number of SSL faults and allows them to be tested in parallel However by reducing the bus size from n to one we can obtain the traditional gate level circuit and models

Lifetime Validation of Digital Systems Via Fault Modeling and Test Generation Hussain Said Al-Asaad, 1998 **Advanced Simulation and Test Methodologies for VLSI Design** G. Russell, I.L. Sayers, 1989-02-28 **Artificial Intelligence And Information-control Systems Of Robots '97 - Proceedings Of The Seventh International Conference** Ivan Plander, 1997-08-12 AIICSR 97 Artificial Intelligence and

Information Control Systems of Robots is one of the most traditional East West professional meetings devoted to artificial intelligence AI and its applications in robots The themes of the conference are aimed at the issues of AI theory and applications The conference is devoted to the development and philosophical reflections of AI and presents the most important topics such as knowledge discovery and data mining and study of context In addition to robots AI has created softbots software robots working in a complex information environment The WWW has become the most exciting application of AI Further important topics in this volume include formal modelling of reactive systems development of parallel and distributed computer architectures declarative programming agent societies and other fields from which theoretical results in computer vision and its applications in robotics deserve special attention [IEEE Circuits & Devices](#) ,1996

Foundations of Software Testing, 2/e Aditya P Mathur,2013 This edition of Foundations of Software Testing is aimed at the undergraduate the graduate students and the practicing engineers It presents sound engineering approaches for test generation ion minimization assessment and enhancement Using numerous examples it offers a lucid description of a wide range of simple to complex techniques for a variety of testing related tasks It also discusses the comparative analyses of commercially available testing tools to facilitate the tool ion **1991 IEEE International Symposium on Circuits and Systems** ,1991 *Register-transfer Level Fault Modeling and Test Evaluation Technique for VLSI Circuits* Pradipkumar Arunbhai Thaker,2000 **Digital Systems Reference Book** Brian Holdsworth,Graham R. Martin,1993 Designed to provide comprehensive coverage of the field of digital systems in a concise but authoritative form For ease of access the book has been divided into five parts fundamentals devices for digital systems system design and techniques system development and applications [13th Symposium on Integrated Circuits and Systems Design](#) Ricardo Augusto da Luz Reis,Jose Carlos Monteiro,Wilhelmus Van Noije,2000 These papers are taken from 13th Brazilian Symposium on Integrated Circuit Design SBCCI 2000 They address issues such as microarchitectures architecture logic design analogue design high level synthesis digital design physical modelling reconfigurable hardware and more [Asian Test Symposium](#) ,2005 **Dissertation Abstracts International** ,2000 *Research Report* ,1987 *Selected Reprints on Logic Design for Testability* Constantin C. Timoc,1984 **Index to IEEE Publications** Institute of Electrical and Electronics Engineers,1998 Issues for 1973 cover the entire IEEE technical literature

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