

Cache memory



The Cache Memory

Peter Norton, John Goodman



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The Cache Memory Book Jim Handy, 1998-01-13 The Second Edition of The Cache Memory Book introduces systems designers to the concepts behind cache design The book teaches the basic cache concepts and more exotic techniques It leads readers through some of the most intricate protocols used in complex multiprocessor caches Written in an accessible informal style this text demystifies cache memory design by translating cache concepts and jargon into practical methodologies and real life examples It also provides adequate detail to serve as a reference book for ongoing work in cache memory design The Second Edition includes an updated and expanded glossary of cache memory terms and buzzwords The book provides new real world applications of cache memory design and a new chapter on cachetricks Illustrates detailed example designs of caches Provides numerous examples in the form of block diagrams timing waveforms state tables and code traces Defines and discusses more than 240 cache specific buzzwords comparing in detail the relative merits of different design methodologies Includes an extensive glossary complete with clear definitions synonyms and references to the appropriate text discussions

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Key Features Illustrates detailed example designs of caches Provides numerous examples in the form of block diagrams timing waveforms state tables and code traces Defines and discusses more than 240 cache specific buzzwords comparing in detail the relative merits of different design methodologies Includes an extensive glossary complete with clear definitions synonyms and references to the appropriate text discussions

Cache and Memory Hierarchy Design Steven A. Przybylski, 1990 A widely read and authoritative book for hardware and software designers This innovative book exposes the characteristics of performance optimal single and multi level cache hierarchies by approaching the cache design process through the novel perspective of minimizing execution time

Official Gazette of the United States Patent and Trademark Office, 2002

Cache-memory Interfaces in Compressed Memory Systems International Business Machines Corporation. Research Division. (IBMRD), Caroline D. Benveniste, Peter A. Franaszek, John T. Robinson, 2000 Abstract We consider a number of cache memory hierarchy design issues in systems with compressed random access memories C RAMs in which compression and decompression occur automatically to and from main memory Using a C RAM as main memory segments of main memory are stored in a compressed format and dynamically decompressed to handle cache misses at the next higher

level of memory Design of main memory directory structures and storage allocation methods in such systems are described elsewhere here we focus on issues related to cache memory interfaces In particular if the cache line size of the cache or caches to which main memory data is transferred is different than the size of the unit of compression in main memory bandwidth and latency problems can occur Another issue is that of guaranteed forward progress that is ensuring that modified lines can be written to the compressed main memory so that the system can continue operation even if overall compression deteriorates We study several approaches for solving these problems using trace driven analysis to evaluate alternatives

The Cache Coherence Problem in Shared-Memory Multiprocessors Igor Tartalja, Veljko Milutinović, 1996-02-13 The book illustrates state of the art software solutions for cache coherence maintenance in shared memory multiprocessors It begins with a brief overview of the cache coherence problem and introduces software solutions to the problem The text defines and details static and dynamic software schemes techniques for modeling performance evaluation mechanisms and performance evaluation studies

Parallel and Distributed Simulation Systems Richard M. Fujimoto, 2000-01-03 From the preface page xv My goal in writing Parallel and Distributed Simulation Systems is to give an in depth treatment of technical issues concerning the execution of discrete event simulation programs on computing platforms composed of many procesores interconnected through a network

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Proceedings Tencon ,1987

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