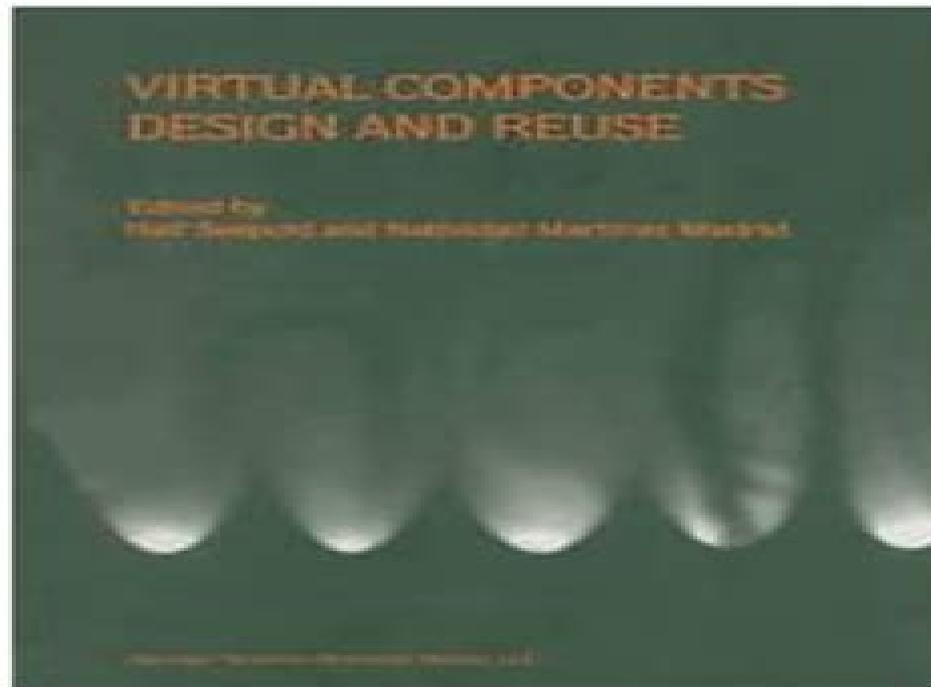


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Virtual Components Design And Reuse

Marcel A. Müller



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Virtual Components Design and Reuse Ralf Seepold, Natividad Martinez Madrid, 2013-06-29 Design reuse is not just a topic of research but a real industrial necessity in the microelectronic domain and thus driving the competitiveness of relevant areas like for example telecommunication or automotive Most companies have already dedicated a department or a central unit that transfer design reuse into reality All main EDA conferences include a track to the topic and even specific conferences have been established in this area both in the USA and in Europe *Virtual Components Design and Reuse* presents a selection of articles giving a mature and consolidated perspective to design reuse from different points of view The authors stem from all relevant areas research and academia IP providers EDA vendors and industry Some classical topics in design reuse like specification and generation of components IP retrieval and cataloguing or interface customisation are revisited and discussed in depth Moreover new hot topics are presented among them IP quality platform based reuse software IP IP security business models for design reuse and major initiatives like the MEDEA EDA Roadmap

Design of Hardware/Software Embedded Systems Eugenio Villar Bonet, 2001 Este libro presenta los desaf os planteados por las nuevas y sumamente poderosas tecnolog as de integraci n de sistemas electr nicos que est n en la base de los cambios sociales hacia lo que llaman la Sociedad de la Informaci n en la que los dispositivos electr nicos se har n una parte incorporada de la vida diaria encajados en casi cada producto Es necesario un conocimiento cuidadoso de los desaf os para aprovechar la amplia gama de ocasiones ofrecidas por tales capacidades de integraci n y las correspondientes posibilidades de dise o de sistemas electr nicos

Reuse Methodology Manual for System-on-a-Chip Designs Pierre Bricaud, 2007-05-08 This revised and updated third edition outlines a set of best practices for creating reusable designs for use in an System on a Chip SoC design methodology These practices are based on the authors experience in developing reusable designs as well as the experience of design teams in many companies around the world

Reuse Techniques for VLSI Design Ralf Seepold, Arno Kunzmann, 2012-12-06 *Reuse Techniques for VLSI Design* is a reflection on the current state of the art in design reuse for microelectronic systems To that end it is the first book to garner the input of leading experts from both research and application areas These experts document herein not only their more mature approaches but also their latest research results Firstly it sets out the background and support from international organisations that enforce System on a Chip SoC design by reuse oriented methodologies This overview is followed by a number of technical presentations covering different requirements of the reuse domain These are presented from different points of view i e IP provider IP user designer isolated reuse intra company or inter company reuse More general systems or case studies e g metrics are followed by comprehensive reuse systems e g reuse management systems partly including business models Since design reuse must not be restricted to digital components mixed signal and analog reuse approaches are also presented In parallel to the digital domain this area covers research in reuse database design Design verification and legal aspects are two

important topics that are closely related to the realization of design reuse These hot topics are covered by presentations that finalize the survey of outstanding research development and application of design reuse for SoC design Reuse Techniques for VLSI Design is an invaluable reference for researchers and engineers involved in VLSI ASIC design *System-on-Chip Methodologies & Design Languages* Peter J. Ashenden, Jean Mermet, Ralf Seepold, 2013-03-14 System on Chip Methodologies the Forum on Design Languages FDL held in Europe and the Asia Pacific Chip Design Language APChDL Conference The papers cover a range of topics including design methods specification and modeling languages tool issues formal verification simulation and synthesis The results presented in these papers will help researchers and practicing engineers keep abreast of developments in this rapidly evolving field Reuse Methodology Manual Pierre Bricaud, 2012-12-06 Silicon technology now allows us to build chips consisting of tens of millions of transistors This technology not only promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer As a result many ASIC developers and silicon vendors are re examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available These designers see current design tools and methodologies as inadequate for developing million gate ASICs from scratch There is considerable pressure to keep design team size and design schedules constant even as design complexities grow Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology Design reuse the use of pre designed and pre verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity Reuse Methodology Manual for System On A Chip Designs Second Edition outlines an effective methodology for creating reusable designs for use in a System on a Chip SoC design methodology Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem Instead this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process Reuse Methodology Manual for System On A Chip Designs Second Edition will be updated on a regular basis as a result of changing technology and improved insight into the problems of design reuse and its role in producing high quality SoC designs **IEEE Circuits & Devices**, 2005 **Reuse Methodology Manual for System-on-a-chip Designs** Michael Keating, Pierre Bricaud, 1999 Silicon technology now allows us to build chips consisting of tens of millions of transistors This technology not only promises new levels of system integration onto a single chip but also presents significant challenges to the chip designer As a result many ASIC developers and silicon vendors are re examining their design methodologies searching for ways to make effective use of the huge numbers of gates now available Design reuse the use of pre designed and pre verified cores is the most promising opportunity to bridge the gap between available gate count and designer productivity Reuse Methodology Manual for System On A Chip Designs Second Edition outlines an effective methodology for creating reusable designs for use in a System on a Chip SoC design methodology Silicon and tool

technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem. Instead, this manual is an attempt to capture and incrementally improve on current best practices in the industry and to give a coherent integrated view of the design process.

Technologies for the Information Society Jean-Yves Roger, Brian Stanford-Smith, Paul T. Kidd, 1998. GATEWAYS TO DEMOCRACY continues with its framework of gateways to help readers conceptualize participation and civic engagement even democracy itself with reference to how individuals access the political system. This approach helps readers better see the relevance of government in their lives. GATEWAYS uniquely incorporates policy into a section at the end of each chapter helping readers better understand the connection between public opinion, policy making, and how public policy applies to their lives. The second edition complete with 2012 election updates emphasizes critical thinking by clearly outlining learning outcomes and enhancing learning with self-assessment Checkpoints and a clear chapter study plan. Chapters in this ESSENTIALS version are condensed to accommodate a shorter format but preserve the integrity of the text's hallmarks.

Proceedings, 2001 Electronic Business, 2001. The management magazine for the electronics industry. **Monolithic and Top-down Clock Synthesis with Micromachined Radio Frequency Reference** Michael Shannon McCorquodale, 2004. *Information Hiding*, 2001. International Symposium on Quality Electronic Design, 2002. Annotation: Fifty-one papers and 21 posters from the March 2002 symposium report current research in deep submicron integrated circuit design and development. The sessions address interconnect extraction and modeling, design for process variations, metrics, power and noise management, verification, signal integrity, and low power design techniques. Some of the topics are: transition aware global signaling, TAGS, the interoperability of EDA tools for sequential logic synthesis, statistical methods for the determination of process corners, power supply noise suppression via clock skew scheduling, and the relation between SAT and BDDs for equivalence checking. No subject index. Annotation copyrighted by Book News Inc, Portland, OR. **Proceedings** VHDL International. Users Forum. Fall Workshop, 1999. Electronic Design, 2000. **Embedded Systems Programming**, 1998-07. *IECON '99* IEEE Industrial Electronics Society. Conference, IEEE Industrial Electronics Society, 1999. This text constitutes proceedings from the Annual Conference of the Industrial Electronics Society, IECON, which took place in 1999. Topics covered include control and signal processing for microlithography, process autonomous mobile robots, and fuzzy logic. **International Conference on VLSI and CAD**, 1999. **Internationalisation of Innovation** Dieter Ernst, 2004.

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