

# AFT

## ARMY FITNESS TEST



The Army Fitness Test (AFT) is the official physical fitness test of record for all Soldiers on June 1, 2025, replacing the Army Combat Fitness Test.

Designed to increase warfighting readiness, reduce injury risk, and enhance the physical performance of the force.

### AFT Events

Three-Repetition  
Maximum Deadlift



Hand-Release  
Push-Up Arm  
Extension



Sprint-Drag-Carry



Plank



Two-Mile Run



**Combat Specialties:** Introduces one sex-neutral, age-normed standard that requires a total score of 350, with a minimum of 60 points per event.

**Combat Enabling Specialties:** Maintains sex- and age-normed scoring that requires a total score of 300.

April 23, 2025

Army Directive  
published on Army  
Publishing  
Directorate:  
<https://armypubs.army.mil/>

May 2025

Execution Order  
published with  
Implementation  
Guidance

June 1, 2025

AFT becomes official  
test of record

Jan. 1, 2026

New scoring  
standards for  
Soldiers in 21 combat  
military occupational  
specialties (MOS)  
take effect for the  
active component

June 1, 2026

New scoring  
standards for  
Soldiers in 21  
combat military  
occupational  
specialties (MOS) for  
the Reserve and  
National Guard

### Combat Specialties

11A. Infantry Officer  
11B. Infantryman  
11C. Indirect Fire Infantryman (Mortarman)  
11Z. Infantry Senior Sergeant  
12A. Engineer, General Engineer  
12B. Combat Engineer  
13A. Field Artillery Officer  
13F. Fire Support Specialist  
18A. Special Forces Officer  
180A. Special Forces Warrant Officer  
18B. Special Forces Weapons Sergeant

18C. Special Forces Engineer Sergeant  
18D. Special Forces Medical Sergeant  
18E. Special Forces Communications Sergeant  
18F. Special Forces Intelligence Sergeant  
18Z. Special Forces Senior Sergeant  
19A. Armor Officer  
19C. Bradley Crew member  
19D. Cavalry Scout  
19K. M1 Armor Crewman  
19Z. Armor Senior Sergeant

Combat Specialties will start prepping for Combat AFT standards after June 1, 2025

For more information  
Scan the QR code.



# Testing For Combat

**N Noddings**



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web apr 7 2014 the vhdl code for full adder circuit adds three one bit binary numbers a b cin and outputs two one bit binary numbers a sum s and a carry cout truth table describes the functionality of full adder sum s output is high when odd number of inputs are high cout is high when two or more inputs are high

and all elements of an n bit array in vhdl stack overflow - Apr 14 2022

web nov 30 2013 lets say i have an n bit array i want to and all elements in the array similar to wiring each element to an n bit and gate how do i achieve this in vhdl note i am trying to use re usable vhdl code so i want to avoid hard coding something like result array 0 and array 1 and array 2 and array n thanks oshara

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web this tutorial describes language features that are common to all versions of the language they are expressed using the syntax of vhdl 93 and subsequent versions there are some aspects of syntax that are incompatible with the original vhdl 87 version however most tools now support at least vhdl 93 so syntactic differences

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web feb 16 2023 by using the coding style above there is no question about which version of bottom is wanted the version in the library my lib1 is the correct one care should be taken when choosing library names for vhdl files while a library called work is a common library name for many projects the tool will handle it a little differently than

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web high level synthesisable vhdl hvhdl is a set of coding patterns for standard vhdl which are designed to greatly increase

abstraction level of vhdl source code using standard synthesis tools the coding patterns are designed to support incremental design testing and development of the vhdl source code

*vhdl tool - Dec 23 2022*

web overview visual studio code is an open source editor from microsoft vhdl tool makes its services available to vs code through the language server protocol vscode plugin find the plugin by searching for vhdl in the extensions sidebar or go to the online marketplace follow the instructions in the readme

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web dec 29 2017 vhdl uses a similar description however it has its own syntax for example it uses the following lines of code to describe the input and output ports of this circuit 1 entity circuit 1 is 2 port a in std logic 3 b in std logic 4 out1 out std logic 5 end circuit 1

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web apr 29 2016 vhdl was created in the 1980s to develop a high speed integrated circuit it has since become an industry standard language for describing digital systems at the structural or behavioral levels in a text based format the vhdl file can be used to manufacture a physical circuit such as a motherboard processor or memory module

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web basic logic gates esd chapter 2 figure 2 3 every vhdl design description consists of at least one entity architecture pair or one entity with multiple architectures the entity section of the hdl design is used to declare the i o ports of the circuit while the description code resides within architecture portion

*lab 6 single clock data path for 16 bit r type instructions in - Jun 16 2022*

web quartus and vhdl code in this section you should learn how to implement a vhdl code for single cycle data path before we go any further let s define some of the terms that we use throughout the book entity all designs are expressed in terms of entities an entity is the most basic building block in a design