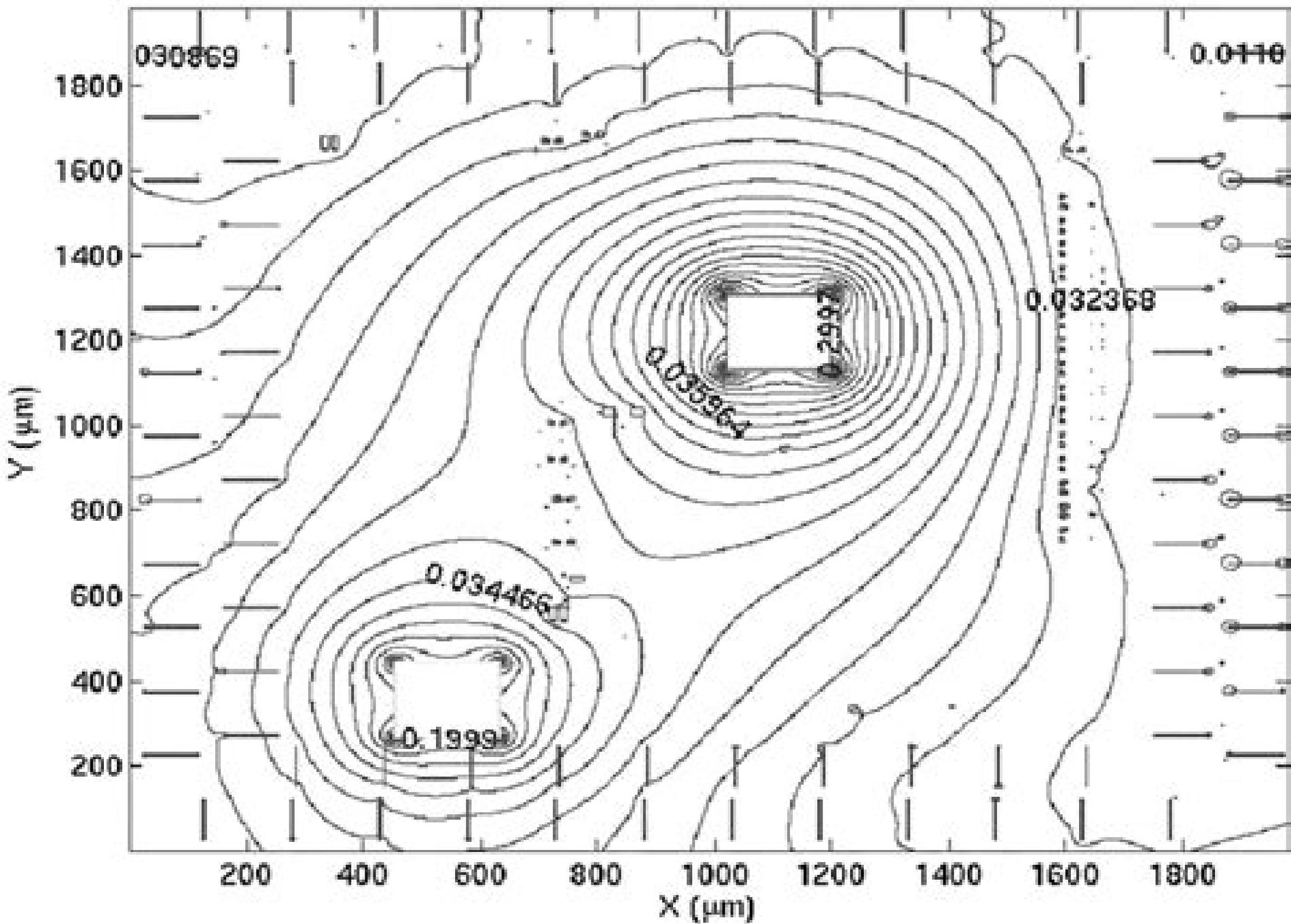


# Surface Substrate Noise Contour



# Substrate Noise

**Krzysztof Iniewski**



## **Substrate Noise:**

**Substrate Noise Coupling in Mixed-Signal ASICs** Stéphane Donnay, Georges Gielen, 2006-05-31 This book is the first in a series of three dedicated to advanced topics in Mixed Signal IC design methodologies It is one of the results achieved by the Mixed Signal Design Cluster an initiative launched in 1998 as part of the TARDIS project funded by the European Commission within the ESPRIT IV Framework This initiative aims to promote the development of new design and test methodologies for Mixed Signal ICs and to accelerate their adoption by industrial users As Microelectronics evolves Mixed Signal techniques are gaining a significant importance due to the wide spread of applications where an analog front end is needed to drive a complex digital processing subsystem In this sense Analog and Mixed Signal circuits are recognized as a bottleneck for the market acceptance of Systems On Chip because of the inherent difficulties involved in the design and test of these circuits Specially problems arising from the use of a common substrate for analog and digital components are a main limiting factor The Mixed Signal Cluster has been formed by a group of 11 Research and Development projects plus a specific action to promote the dissemination of design methodologies techniques and supporting tools developed within the Cluster projects The whole action ending in July 2002 has been assigned an overall budget of more than 8 million EURO

Substrate Noise Edoardo Charbon, Ranjit Gharpurey, Paolo Miliozzi, Robert G. Meyer, Alberto L.

Sangiovanni-Vincentelli, 2007-05-08 In the past decade substrate noise has had a constant and significant impact on the design of analog and mixed signal integrated circuits Only recently with advances in chip miniaturization and innovative circuit design has substrate noise begun to plague fully digital circuits as well To combat the effects of substrate noise heavily over designed structures are generally adopted thus seriously limiting the advantages of innovative technologies Substrate Noise Analysis and Optimization for IC Design addresses the main problems posed by substrate noise from both an IC and a CAD designer perspective The effects of substrate noise on performance in digital analog and mixed signal circuits are presented along with the mechanisms underlying noise generation injection and transport Popular solutions to the substrate noise problem and the trade offs often debated by designers are extensively discussed Non traditional approaches as well as semi automated techniques to combat substrate noise are also addressed Substrate Noise Analysis and Optimization for IC Design will be of interest to researchers and professionals interested in signal integrity as well as to mixed signal and RF designers

*Substrate Noise Coupling in Analog/RF Circuits* Stephane Bronckers, Geert Van der Plas, Gerd Vandersteen, Yves Rolain, 2010 This book presents case studies to illustrate that careful modeling of the assembly characteristics and layout details is required to bring simulations and measurements into agreement Engineers learn how to use a proper combination of isolation structures and circuit techniques to make analog RF circuits more immune to substrate noise Topics include substrate noise propagation passive isolation structures noise couple in active devices measuring the coupling mechanisms in analog RF circuits prediction of the impact of substrate noise on analog RF circuits and noise

coupling in analog RF systems      *Substrate Noise Coupling in RFICs* Ahmed Helmy, Mohammed Ismail, 2008-03-23 The book reports modeling and simulation techniques for substrate noise coupling effects in RFICs and introduces isolation structures and design guides to mitigate such effects with the ultimate goal of enhancing the yield of RF and mixed signal SoCs The book further reports silicon measurements and new test and noise isolation structures To the authors knowledge this is the first title devoted to the topic of substrate noise coupling in RFICs as part of a large SoC

*Substrate Noise* Edoardo Charbon, Ranjit Gharpurey, Paolo Miliozzi, 2014-01-15      *Characterization of Substrate Noise Coupling, Its Impacts and Remedies in RF and Mixed-signal ICs* Ahmed Helmy, 2006 Abstract Substrate noise coupling in integrated circuits is the process by which interference signals generated by high speed digital blocks cause parasitic currents to flow in the silicon substrate and couple devices in various parts of the circuits on this common substrate In RFIC the switching noise couples to the sensitive analog circuits through the substrate causing degradation in performance and yield hit Overcoming substrate coupling is a key issue in successful system on chip integration In this thesis a substrate aware design flow is built calibrated to silicon and used as part of the design flow to uncover substrate coupling problems in RFICs in the design phase The flow is used to develop the first comprehensive RF substrate noise isolation design guide to be used by RF designers during the design phase This will allow designers to optimize the design to maximize noise isolation and protect sensitive blocks from being degraded by substrate noise coupling Several effects of substrate coupling on circuit performance will be identified and remedies will be given based on the design guide Three case studies are designed to analyze the substrate coupling problem in RFICs The case studies are designed to attack the problem from the device circuit and system levels On the device level a special emphasis is given to designing on chip inductors as an important device in RFIC An accurate model is developed for a broadband fit of the inductor scattering parameters This model is shown to be scalable and is proven to be accurate across various frequency bands and geometries A special emphasis is put on the design for manufacturing effects that affect the design robustness A circuit level case study is developed and results are compared to simulations and measurements to highlight the need for such a flow before tapping out to ensure a yielding part The system level problem studied is a GSM receiver where the research results are directly applied to it as a demonstration vehicle to debug and resolve a system level substrate noise coupling problem that otherwise caused a product to be on the edge of malfunction

*Noise Coupling in System-on-Chip* Thomas Noulis, 2018-01-09 Noise Coupling is the root cause of the majority of Systems on Chip SoC product fails The book discusses a breakthrough substrate coupling analysis flow and modelling toolset addressing the needs of the design community The flow provides capability to analyze noise components propagating through the substrate the parasitic interconnects and the package Using this book the reader can analyze and avoid complex noise coupling that degrades RF and mixed signal design performance while reducing the need for conservative design practices With chapters written by leading international experts in the field novel methodologies are provided to identify noise

coupling in silicon It additionally features case studies that can be found in any modern CMOS SoC product for mobile communications automotive applications and readout front ends

**Substrate Noise Analysis in RF Integrated Circuits**, 2004 Substrate coupling in integrated circuits is the process whereby parasitic current flow in the substrate electrically couples devices in different parts of the circuit Higher levels of integration and higher frequencies of operation makes the coupling more pronounced in modern circuit realizations Electrical coupling in the substrate leads to undesirable interaction between devices which can degrade circuit performance The degradation can manifest itself in different ways In mixed analog digital circuits for example the switching noise generated by digital circuits can be coupled to sensitive analog circuits through the substrate Performance degradation due to substrate coupling can be addressed at the circuit design stage by including substrate models in circuit analysis Analytical models based on simple substrate resistance plots are developed Trends in substrate resistance variation for different substrates are studied to understand its effect at the circuit level Analytical model for measurement of substrate coupling at the circuit level based on substrate resistance information and other circuit parameters is developed Efficient techniques to improve isolation based on simulation and analysis of the substrate model are discussed

**Substrate Noise in Mixed-signal Integrated Circuits** Min Xu, 2001 **Analysis of Substrate Noise Coupling in Mixed Signal Integrated Circuits** Cole Erwin Zemke, 2003 [Substrate Noise Analysis in RF Integrated Circuits](#) Ravi C. Vijayaraghavan, 2003 Keywords Isolation Analysis SUBstrate Noise Analytical Model of Coupling

**Signal Integrity Effects in Custom IC and ASIC Designs** Raminderpal Singh, 2001-12-12 offers a tutorial guide to IC designers who want to move to the next level of chip design by unlocking the secrets of signal integrity Jake Buurma Senior Vice President Worldwide Research Development Cadence Design Systems Inc Covers signal integrity effects in high performance Radio Frequency RF IC Brings together research papers from the past few years that address the broad range of issues faced by IC designers and CAD managers now and in the future A Wiley IEEE Press publication

**Modeling of Substrate Noise Coupling in Mixed-signal Integrated Circuits** Nawej Mwez, 2002 **Microwave and Millimeter Wave Circuits and Systems** Apostolos Georgiadis, Hendrik Rogier, Luca Roselli, Paolo Arcioni, 2012-09-17 Microwave and Millimeter Wave Circuits and Systems Emerging Design Technologies and Applications provides a wide spectrum of current trends in the design of microwave and millimeter circuits and systems In addition the book identifies the state of the art challenges in microwave and millimeter wave circuits systems design such as behavioral modeling of circuit components software radio and digitally enhanced front ends new and promising technologies such as substrate integrated waveguide SIW and wearable electronic systems and emerging applications such as tracking of moving targets using ultra wideband radar and new generation satellite navigation systems Each chapter treats a selected problem and challenge within the field of Microwave and Millimeter wave circuits and contains case studies and examples where appropriate Key Features Discusses modeling and design strategies for new appealing applications in the domain of microwave and millimeter wave

circuits and systems Written by experts active in the Microwave and Millimeter Wave frequency range industry and academia Addresses modeling design applications both from the circuit as from the system perspective Covers the latest innovations in the respective fields Each chapter treats a selected problem and challenge within the field of Microwave and Millimeter wave circuits and contains case studies and examples where appropriate This book serves as an excellent reference for engineers researchers research project managers and engineers working in R D professors and post graduates studying related courses It will also be of interest to professionals working in product development and PhD students

**Substrate Noise Analysis and Techniques for Mitigation in Mixed-signal RF Systems** Nisha Checka,2005 Cont Existing techniques have prohibitively long simulation times and are only suitable for final verification Determination of substrate noise coupling during the design phase would be extremely beneficial to circuit designers who can incorporate the effect of the noise and re design accordingly before fabrication This would reduce the turn around time for circuits and prevent costly redesign SNAT can be used at any stage of the design cycle to accurately predict less than 12% error when compared to measurements the substrate noise performance of any digital circuit with a large degree of computational efficiency

*Wireless Technologies* Krzysztof Iniewski,2017-12-19 Advanced concepts for wireless technologies present a vision of technology that is embedded in our surroundings and practically invisible From established radio techniques like GSM 802 11 or Bluetooth to more emerging technologies such as Ultra Wide Band and smart dust motes a common denominator for future progress is the underlying integrated circuit technology Wireless Technologies responds to the explosive growth of standard cellular radios and radically different wireless applications by presenting new architectural and circuit solutions engineers can use to solve modern design problems This reference addresses state of the art CMOS design in the context of emerging wireless applications including 3G 4G cellular telephony wireless sensor networks and wireless medical application Written by top international experts specializing in both the IC industry and academia this carefully edited work uncovers new design opportunities in body area networks medical implants satellite communications automobile radar detection and wearable electronics The book is divided into three sections wireless system perspectives chip architecture and implementation issues and devices and technologies used to fabricate wireless integrated circuits Contributors address key issues in the development of future silicon based systems such as scale of integration ultra low power dissipation and the integration of heterogeneous circuit design style and processes onto one substrate Wireless sensor network systems are now being applied in critical applications in commerce healthcare and security This reference which contains 25 practical and scientifically rigorous articles provides the knowledge communications engineers need to design innovative methodologies at the circuit and system level

**Substrate Noise Coupling in Ring Oscillator-based Phase Locked Loops** Robert Shreeve,2009 In this thesis the performance degradation of a phase locked loop due to substrate noise is examined A new analytical equivalent circuit model for substrate noise coupling is derived for a heavily doped silicon substrate The model has been

validated with measured data from a 0.35  $\mu\text{m}$  CMOS process. Since the model is physical, it can be used to predict substrate noise coupling without the need for extensive computer simulations using three-dimensional finite difference or Green's function solvers. This is followed by an evaluation of the effect of substrate noise in a PLL. A PLL test chip fabricated in a 0.13  $\mu\text{m}$  CMOS process has been characterized over a wide range of substrate noise frequencies. The measured results combined with extensive simulations provide insight into the mechanisms for noise coupling in a PLL. Based on an understanding of the noise coupling guidelines for minimizing the impact of substrate noise, are presented.

**The Computer Engineering Handbook** Vojin G. Oklobdzija, 2001-12-26. There is arguably no field in greater need of a comprehensive handbook than computer engineering. The unparalleled rate of technological advancement, the explosion of computer applications, and the now-in-progress migration to a wireless world have made it difficult for engineers to keep up with all the developments in specialties outside their own. References published only a few years ago are now sorely out of date. The Computer Engineering Handbook changes all of that. Under the leadership of Vojin Oklobdzija and a stellar editorial board, some of the industry's foremost experts have joined forces to create what promises to be the definitive resource for computer design and engineering. Instead of focusing on basic introductory material, it forms a comprehensive state-of-the-art review of the field's most recent achievements, outstanding issues, and future directions. The world of computer engineering is vast and evolving so rapidly that what is cutting edge today may be obsolete in a few months. While exploring the new developments, trends, and future directions of the field, The Computer Engineering Handbook captures what is fundamental and of lasting value.

**Suppression of Substrate Noise in a Mixed-signal CMOS Integrated Circuit** Wei Tjan (Richard) Lim, 1996. Substrate switching noise is becoming a concern as integrated circuits get larger and speeds get faster. Mixed-mode integrated circuits are especially affected as the substrate noise interferes with sensitive analog circuits, resulting in limited signal-to-noise ratios. This thesis serves to study the cause of the noise at the point where it is generated, to the way it propagates to the analog circuits, and presents several approaches to reduce the switching noise. In addition, it examines the substrate impedance as being a key element to successful and reliable design for low-noise CMOS mixed-signal integrated circuits. Utilizing the substrate lead inductance and current-variable capacitances through the use of guard ring diodes, resonant frequencies which provide a low impedance path to ground are created. These can be tuned to coincide with problematic noise frequency components or to cancel the pin and package resonance, thus suppressing noise and improving reliability.

**Digital Design and Fabrication** Vojin G. Oklobdzija, 2017-12-19. In response to tremendous growth and new technologies in the semiconductor industry, this volume is organized into five information-rich sections. Digital Design and Fabrication surveys the latest advances in computer architecture and design, as well as the technologies used to manufacture and test them. Featuring contributions from leading experts, the book also includes a new section on memory and storage, in addition to a new chapter on nonvolatile memory technologies. Developing advanced concepts, this sharply focused book

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