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# **Wave Pipelining: Theory and CMOS Implementation**

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**C. Thomas Gray  
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**Springer Science+Business Media, LLC**

# Wave Pipelining Theory And Cmos Implementation

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## **Wave Pipelining Theory And Cmos Implementation:**

**Wave Pipelining: Theory and CMOS Implementation** C. Thomas Gray, Wentai Liu, Ralph K. Cavin, III, 2012-12-06 The quest for higher performance digital systems for applications such as general purpose computing signal image processing and telecommunications and an increasing cost consciousness have led to a major thrust for high speed VLSI systems implemented in inexpensive and widely available technologies such as CMOS This monograph based on the first author's doctoral dissertation concentrates on the technique of wave pipelining as one method toward achieving this goal The primary focus of this monograph is to provide a coherent presentation of the theory of wave pipelined operation of digital circuits and to discuss practical design techniques for the realization of wave pipelined circuits in the CMOS technology Wave pipelining can be applied to a variety of circuits for increased performance For example many architectures that support systolic computation lend themselves to wave pipelined realization Also the wave pipeline design methodology emphasizes the role of controlled clock skew in extracting enhanced performance from circuits that are not deeply pipelined Wave pipelining also known as maximal rate pipelining is a timing methodology used in digital systems to increase the number of effective pipeline stages without increasing the number of physical registers in the pipeline Using this technique new data is applied to the inputs of a combinational logic block before the outputs due to previous inputs are available thus effectively pipelining the combinational logic and maximizing the utilization of the logic *High Performance Clock Distribution Networks* Eby G. Friedman, 2012-12-06 A number of fundamental topics in the field of high performance clock distribution networks is covered in this book High Performance Clock Distribution Networks is composed of ten contributions from authors at academic and industrial institutions Typically these contributions can be grouped within three primary areas The first topic area deals with exploiting the localized nature of clock skew The second topic area deals with the implementation of these clock distribution networks while the third topic area considers more long range aspects of next generation clock distribution networks High Performance Clock Distribution Networks presents a number of interesting strategies for designing and building high performance clock distribution networks Many aspects of the ideas presented in these contributions are being developed and applied today in next generation high performance microprocessors *Clock Distribution Networks in VLSI Circuits and Systems* Eby G. Friedman, 1995 Improve the performance and reliability of synchronous digital integrated circuits with this anthology of key literature on the design and analysis of clock distribution networks for VLSI based computer and signal processing systems Beginning with an extensive tutorial overview and bibliography this all in one source offers substantive coverage of the most relevant issues related to the design of clock distribution networks for application to high performance synchronous design Related topics include clock skew automated layout of clock nets distributed buffer and interconnect delays clock distribution design of structured custom VLSI circuits wafer scale integration systolic arrays globally asynchronous locally synchronous systems microwave issues low power

clocking techniques process insensitive circuits deterministic and probabilistic delay models system timing specifications clock distribution networks of well known circuits and future research in clock distribution networks The material presented in Clock Distribution Networks in VLSI Circuits and Systems will be valuable to anyone with an interest in synchronous integrated circuits computer design or signal processing implementation issues

**Digital Systems Engineering** William J. Dally, John W. Poulton, 2008-04-24 What makes some computers slow Why do some digital systems operate reliably for years while others fail mysteriously every few hours How can some systems dissipate kilowatts while others operate off batteries These questions of speed reliability and power are all determined by the system level electrical design of a digital system Digital Systems Engineering presents a comprehensive treatment of these topics It combines a rigorous development of the fundamental principles in each area with real world examples of circuits and methods The book not only serves as an undergraduate textbook filling the gap between circuit design and logic design but can also help practising digital designers keep pace with the speed and power of modern integrated circuits The techniques described in this book once used only in supercomputers are essential to the correct and efficient operation of any type of digital system

Low-power HF Microelectronics Gerson A. S. Machado, 1996 This book brings together innovative modelling simulation and design techniques in CMOS SOI GaAs and BJT to achieve successful high yield manufacture for low power high speed and reliable by design analogue and mixed mode integrated systems

**Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology**, 1997

**The Electrical Engineering Handbook** Wai Kai Chen, 2004-11-16 The Electrical Engineer's Handbook is an invaluable reference source for all practicing electrical engineers and students Encompassing 79 chapters this book is intended to enlighten and refresh knowledge of the practicing engineer or to help educate engineering students This text will most likely be the engineer's first choice in looking for a solution extensive complete references to other sources are provided throughout No other book has the breadth and depth of coverage available here This is a must have for all practitioners and students The Electrical Engineer's Handbook provides the most up to date information in Circuits and Networks Electric Power Systems Electronics Computer Aided Design and Optimization VLSI Systems Signal Processing Digital Systems and Computer Engineering Digital Communication and Communication Networks Electromagnetics and Control and Systems About the Editor in Chief Wai Kai Chen is Professor and Head Emeritus of the Department of Electrical Engineering and Computer Science at the University of Illinois at Chicago He has extensive experience in education and industry and is very active professionally in the fields of circuits and systems He was Editor in Chief of the IEEE Transactions on Circuits and Systems Series I and II President of the IEEE Circuits and Systems Society and is the Founding Editor and Editor in Chief of the Journal of Circuits Systems and Computers He is the recipient of the Golden Jubilee Medal the Education Award and the Meritorious Service Award from the IEEE Circuits and Systems Society and the Third Millennium Medal from the IEEE Professor Chen is a fellow of the IEEE and the American Association for the

Advancement of Science 77 chapters encompass the entire field of electrical engineering THOUSANDS of valuable figures tables formulas and definitions Extensive bibliographic references

**Clock Tree Synthesis for Low Power IC Design** Gufeng Xi,1996

**Design of Ultrafast Digital Circuits Using Quantum Electronic Devices** Sundararajarao Mohan,1995

**Performance Optimization of Pipeline Circuits with Latches and Wave Pipelining** Chuan-Hua Chang,1996

*Asymptotic Waveform Evaluation* Eli Chiprout,Michel S. Nakhla,1994 The intense drive for signal integrity has been at the forefront of rapid and new developments in CAD algorithms With increasing demands for high signal speeds coupled with a decrease in feature size interconnect effects such as signal delay distortion and crosstalk become the dominant factor limiting overall performance of VLSI systems Although SPICE is used on a daily basis by many engineers for analog simulation and general circuit analysis current versions of SPICE do not handle adequately the new emerging challenges of interconnect effects Moment matching techniques such as asymptotic waveform evaluation have recently proven useful in the analysis of large interconnect structures containing elements such as lossy coupled transmission lines with linear or nonlinear terminations At a CPU cost of a little more than one DC analysis these techniques are 2 3 orders of magnitude faster than full simulation techniques such as FFT Asymptotic Waveform Evaluation presents an overview of the diverse algorithms and applications of moment matching techniques The material is presented systematically and is supported by many examples Issues such as sensitivity analysis and three dimensional analysis are also covered Asymptotic Waveform Evaluation will be of interest to engineers students and researchers involved in the development and study of circuit simulation as well as interconnect analysis It will also interest design engineers who are involved in dealing with high speed issues and graduate students who are active in the development of CAD tools for electronic systems

**Formal Semantics for VHDL** Carlos Delgado Kloos,P. Breuer,1995-02-28 Research papers from a January 1994 workshop put forth a cohesive set of semantics for the VHDL language and describe semantics based on Petri nets as target language higher order logic functional concepts and evolving algebras Quotes from Lewis Carroll s Alice Through the Looking Glass introduce each paper For researchers in formal methods and advanced students No index Annotation copyright by Book News Inc Portland OR

Digital Timing Macromodeling for VLSI Design Verification Jeong-Taek Kong,David V. Overhauser,1995-05-31 Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques It presents detailed discussion of the various techniques implemented in circuit timing fast timing switch level timing switch level and gate level simulation It also discusses mixed mode simulation and interconnection analysis methods The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in existing digital MOS macromodels Specifically the techniques address the device model detail transistor coupling capacitance

effective channel length modulation series transistor reduction effective transconductance input terminal dependence gate parasitic capacitance the body effect the impact of parasitic RC interconnects and the effect of transmission gates The techniques address major sources of errors in existing macromodeling techniques which must be addressed if macromodeling is to be accepted in commercial CAD tools by chip designers The techniques presented in Chapters 4 6 can be implemented in other macromodels and are demonstrated using the macromodel presented in Chapter 3 The new techniques are validated over an extremely wide range of operating conditions much wider than has been presented for previous macromodels thus demonstrating the wide range of applicability of these techniques **Proceedings** ,2001

**Hardware Optimizations Enabled by a Decoupled Fetch Architecture** Glenn Reinman,2001 **1994 IEEE International Symposium on Circuits and Systems** ,1994 Pipelining of IIR Lattice and Wave Digital Filters Jin-Gyun Chung,1994 Node-covering Methodologies for Fault Tolerance in Iterative Logic Structures Francis Marion Hanchek,1997 **Advanced Metallization Conference in ...** ,2006 **Advanced Computer Arithmetic Design** Michael J. Flynn,Stuart F. Oberman,2001 Innovative techniques and cutting edge research in computer arithmetic design Computer arithmetic is a fundamental discipline that drives many modern digital technologies High performance VLSI implementations of 3 D graphics encryption streaming digital audio and video and signal processing all require fast and efficient computer arithmetic algorithms The demand for these fast implementations has led to a wealth of new research in innovative techniques and designs Advanced Computer Arithmetic Design is the result of ten years of effort at Stanford University under the Sub Nanosecond Arithmetic Processor SNAP project which author Michael Flynn directs Written with computer designers and researchers in mind this volume focuses on design rather than on other aspects of computer arithmetic such as number systems representation or precision Each chapter begins with a review of conventional design approaches analyzes the possibilities for improvement and presents new research that advances the state of the art The authors present new data in these vital areas Addition and the Ling adder Improvements to floating point addition Encoding to reduce execution times for multiplication The effects of technology scaling on multiplication Techniques for floating point division Approximation techniques for high level functions such as square root logarithms and trigonometric functions Assessing cost performance of arithmetic units Clocking to increase computer operation frequency New implementation of continued fractions to the approximation of functions This volume presents the results of a decade s research in innovative and progressive design techniques Covering all the most important research topics in the field Advanced Computer Arithmetic Design is the most up to date and comprehensive treatment of new research currently available

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