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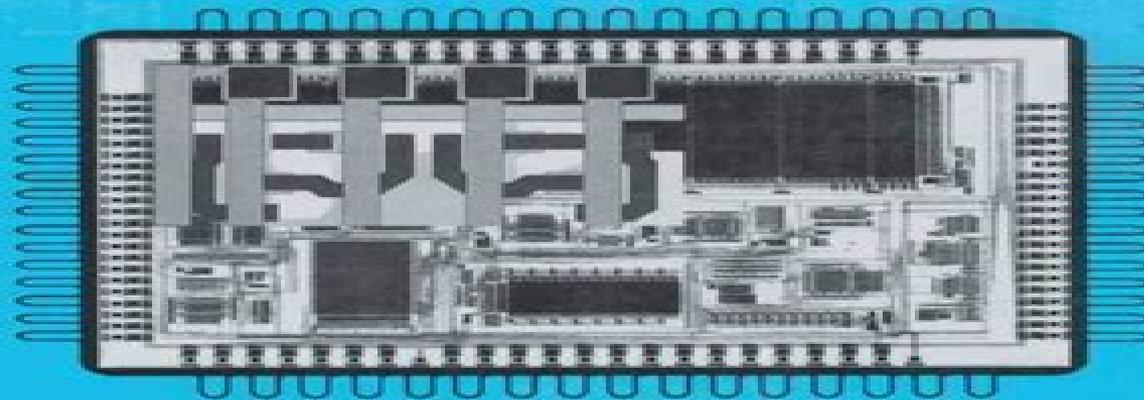
# Testability Concepts for Digital ICs

## The Macro Test Approach

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F.P.M. Beenker  
R.G. Bennetts  
A.P. Thijssen

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# Testability Concepts For Digital Ics The Macro Test Approach

**Jin-Ying Zhang**



## **Testability Concepts For Digital Ics The Macro Test Approach:**

Testability Concepts for Digital ICs F.P.M. Beenker,R.G. Bennetts,A.P. Thijssen,2012-12-06 Preface Testing Integrated Circuits for manufacturing defects includes four basic disciplines First of all an understanding of the origin and behaviour of defects Secondly knowledge of IC design and IC design styles Thirdly knowledge of how to create a test program for an IC which is targeted on detecting these defects and finally understanding of the hardware Automatic Test Equipment to run the test on All four items have to be treated managed and to a great extent integrated before the term IC quality gets a certain meaning and a test a certain measurable value The contents of this book reflects our activities on testability concepts for complex digital ICs as performed at Philips Research Laboratories in Eindhoven The Netherlands Based on the statements above we have worked along a long term plan which was based on four pillars 1 The definition of a test methodology suitable for future IC design styles 2 capable of handling improved defect models 3 supported by software tools and 4 providing an easy link to Automatic Test Equipment The reasoning we have followed was continuously focused on IC qUality Quality expressed in terms of the ability of delivering a customer a device with no residual manufacturing defects Bad devices should not escape a test The basis of IC quality is a thorough understanding of defects and defect models

**Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits** M. Bushnell,Vishwani Agrawal,2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device techn ogy circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signalsubsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers

**Testability Concepts for Digital ICs** Franciscus Petrus Maria Beenker,1994

**SOC (System-on-a-Chip) Testing for Plug and Play Test Automation** Krishnendu Chakrabarty,2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is

seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOCs is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing *Digital Design and Fabrication* Vojin G. Oklobdzija, 2017-12-19 In response to tremendous growth and new technologies in the semiconductor industry this volume is organized into five information rich sections Digital Design and Fabrication surveys the latest advances in computer architecture and design as well as the technologies used to manufacture and test them Featuring contributions from leading experts the book also includes a new section on memory and storage in addition to a new chapter on nonvolatile memory technologies Developing advanced concepts this sharply focused book Describes new technologies that have become driving factors for the electronic industry Includes new information on semiconductor memory circuits whose development best illustrates the phenomenal progress encountered by the fabrication and technology sector Contains a section dedicated to issues related to system power consumption Describes reliability and testability of computer systems Pinpoints trends and state of the art advances in fabrication and CMOS technologies Describes performance evaluation measures which are the bottom line from the user's point of view Discusses design techniques used to create modern computer systems including high speed computer arithmetic and high frequency design timing and clocking and PLL and DLL design

**High-level Test Synthesis of Digital VLSI Circuits** Mike Tien-Chien Lee, 1997 Here is the first book to propose HTS as a complete more effective design approach the author explains how HTS unlike most existing high level synthesis techniques that optimize the circuit architecture for area and performance only is able to explore the synthesis freedom provided at high level to derive an inherently testable architecture at low or even no overhead By permitting testing from the earliest design stages to minimize or even eliminate serious testing problems HTS boosts design quality and shortens the development cycle 17th IEEE VLSI Test Symposium, 1999 The theme of the April 1999 symposium Scaling deeper to submicron test technology challenges reflects the issues being created by the move toward nanometer technologies Many creative and novel ideas and approaches to the current and future electronic circuit testing related problems are explored *IEEE 2000 First International Symposium on Quality Electronic Design*, 2000 European Test Workshop 1999 Hans-Joachim Wunderlich, 1999 Annotation This proceedings contains extended version of a selected subset of the contributions presented at the May 1999 IEEE workshop The 27 papers share research and development RandD results in electronic testing Topics include calculating efficient LFSR seeds for built in self test functional and structural testing of switched current circuits compaction of IDDQ test sequence using reassignment method debug facilities in the TriMedia CPU64 architecture deterministic BIST with

partial scan and using the BS register for capturing and storing n bit sequences in real time Other papers address MEMs switched capacitors ATPG and fault modeling fault simulation and fault coverage of analog circuits FPGAs and regular arrays and low power BIST No subject index Annotation copyrighted by Book News Inc Portland OR

**Proceedings, International Test Conference 1997**, 1997 **11th Asian Test Symposium (ATS'02)**, 2002 Held in Guam in November of 2002 the symposium on the test technologies and research issues related to silicon chip production resulted in the 74 papers presented here The papers are organized into sections related to the symposium sessions on test generation on line testing analog and mixed si

Subject Guide to Children's Books in Print 1997 Bowker Editorial Staff, R R Bowker Publishing, 1996-09 **18th International Conference on VLSI Design** International Conference on VLSI Design, 2005 Asian Test Symposium, 2002 2000 22nd International Conference on Microelectronics IEEE Electron Devices Society, International Conference on Microelectronics, 1999 The papers in this volume are a partial selection from the International Conference on Microelectronic 1999 which provides a forum for the presentation and discussion of the recent developments and future trends in the field of microelectronics

Science Abstracts, 1995 **American Book Publishing Record**, 1996 IEEE VLSI Test Symposium, 2000 **Efficient Testability Design Methodology for Analog/mixed Signal Integrated Circuits** Cheng-Ping Wang, 1997 **Test and Design-for-Testability in Mixed-Signal Integrated Circuits** Jose Luis Huertas Díaz, 2010-02-23 Test and Design for Testability in Mixed Signal Integrated Circuits deals with test and design for test of analog and mixed signal integrated circuits Especially in System on Chip SoC where different technologies are intertwined analog digital sensors RF test is becoming a true bottleneck of present and future IC projects Linking design and test in these heterogeneous systems will have a tremendous impact in terms of test time cost and proficiency Although it is recognized as a key issue for developing complex ICs there is still a lack of structured references presenting the major topics in this area The aim of this book is to present basic concepts and new ideas in a manner understandable for both professionals and students Since this is an active research field a comprehensive state of the art overview is very valuable introducing the main problems as well as the ways of solution that seem promising emphasizing their basis strengths and weaknesses In essence several topics are presented in detail First of all techniques for the efficient use of DSP based test and CAD test tools Standardization is another topic considered in the book with focus on the IEEE 1149.4 Also addressed in depth is the connecting design and test by means of using high level behavioural description techniques specific examples are given Another issue is related to test techniques for well defined classes of integrated blocks like data converters and phase locked loops Besides these specification driven testing techniques fault driven approaches are described as they offer potential solutions which are more similar to digital test methods Finally in Design for Testability and Built In Self Test two other concepts that were taken from digital design are introduced in an analog context and illustrated for the case of integrated filters In summary the purpose of this book is to provide a glimpse on recent

research results in the area of testing mixed signal integrated circuits specifically in the topics mentioned above Much of the work reported herein has been performed within cooperative European Research Projects in which the authors of the different chapters have actively collaborated It is a representative snapshot of the current state of the art in this emergent field

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